

Summary of my research and teaching activities

Personal data	<p>Guy GOGNIAT Born July 17th, 1970 in Palaiseau (91) French nationality 42 years old, married, 2 children</p>
Laboratory	<p>Laboratory Lab-STICC CNRS UMR 6285, University of Bretagne-Sud – UEB</p>
Curriculum Vitae	<p>Current position</p> <ul style="list-style-type: none"> • Professor at University of Bretagne-Sud <i>Teaching activities at University of Bretagne-Sud, Department of Electrical and Computer Engineering Research at Laboratory des Sciences et Techniques de l'Information, de la Communication et de la Connaissance (Lab-STICC)</i> <p>Education</p> <ul style="list-style-type: none"> • Research habilitation University of Bretagne-Sud <i>Graduated - October 26th, 2007</i> • D.Sc. in Electrical Engineering University of Nice – Sophia Antipolis <i>Outstanding thesis award, graduated - November 27th, 1997</i> • M.Sc. in Electrical Engineering University of Paris Sud Orsay <i>Graduated - September 1994</i> • Diploma of engineer in Electrical Engineering University of Paris Sud Orsay <i>Graduated - September 1994</i> <p>Professional experiences</p> <ul style="list-style-type: none"> • September 2009/Today Professor at University of Bretagne-Sud • September 2005/August 2009 Associate Professor at University of Bretagne-Sud • November 2004/August 2005 Invited Researcher (CRCT – Grant ERE DGA) <i>Department of Electrical and Computer Engineering, University of Massachusetts, Amherst, MA, USA</i> • September 1998/October 2004 Associate Professor at University of Bretagne Sud • September 1997/ August 1998 Assistant Professor University of Nice – Sophia Antipolis • September 1994/ August 1997 Teaching Assistant University of Nice – Sophia Antipolis • September 1994/ August 1997 PhD Student (Grant MENRT) <i>Laboratory I3S, CNRS – University of Nice – Sophia Antipolis</i>
Teaching keywords	<p>Digital and analog design, ASIC design, FPGA/CPLD, VHDL, C, cryptography, processors, microcontroller, codesign, adaptive systems, control systems, programmable automata, industrial and data communication networks, data acquisition, physics of semi-conductors, specification languages for embedded systems (Esterel, SystemC, VHDL-AMS...)</p>
Teaching activities	<p>L2 level – Field of electrical and computer engineering L3 level – Field of electrical and computer engineering M1 level – Field of electrical and computer engineering M2 level – Field of electrical and computer engineering and cryptography</p>
Publications related to teaching activities	<p>2 publications en international conferences</p>
Research keywords	<p>Codesign, partial and dynamic reconfigurable architectures, self partial reconfiguration of FPGAs, security of embedded systems (memory protection), functional partitioning, optimization, synthesis design flow, architecture of embedded systems, MPSoC, hardware/software integration, system level estimation, hardware and software, design space exploration, partitioning, RTOS, telecommunication applications, multimedia et cryptography, Model driven design methodologies (MDA)</p>
Research awards	<p>PEDR Outstanding research award (PEDR 2003/2007) PEDR Outstanding research award (PEDR 2007/2011)</p>
Advising	<p>17 Ph.D. students (11 graduated) 2 Post-Doc 17 M.S. students</p>
Ph. D. Thesis	<p>43 Ph. D. Thesis committee: - 2 as a Member (University of Nice – Sophia Antipolis, University of Bretagne-Sud)</p>

committee	<p>- 10 as an Adviser (University of Bretagne-Sud)</p> <p>- 28 as a Reviewer (University Montpellier II, University of Rennes I, Institut National des Sciences Appliquées de Rennes, Institut Polytechnique de Grenoble, University of Sciences and technology of Lille, University of cergy Pontoise, University of Pierre et Marie Curie...).</p> <p>- 8 as a Chair (Télécom Bretagne, Université de Bretagne Occidentale, Université de Rennes I...)</p>																
Professional service	<p>Steering committee of international workshops <i>CryptArchi 2008, DASIP (2009, 2010, 2011, 2012)</i></p> <p>Program chair of international conferences <i>DASIP 2007, ReCoSoC 2012</i></p> <p>Organization committee member of international conferences <i>DASIP (2008,2009, 2010, 2011, 2012), CryptArchi 2008</i></p> <p>Organization of special session <i>DASIP 2009, ReCoSoC 2011</i></p> <p>Program committee member of international conferences <i>ERSA (2006, 2007, 2008, 2009, 2010, 2011, 2012), DASIP (2007, 2008, 2009, 2010, 2011, 2012), IEEE ISVLSI 2008, CryptArchi (2008, 2009, 2010, 2011), C&ESAR 2008, IEEE IDT (2008, 2009), ReConFig (2008, 2009, 2010, 2011, 2012), IEEE FCCM (2009, 2010, 2011, 2012), ARC (2009, 2010, 2011, 2012), WESS (2010, 2011), RAW (2011,2012), CHANGE 2011, IEEE FPT (2011,2012), ICECS (2011)</i></p> <p>Review committee member of international conferences <i>ERSA 2002, FPL 2003, IEEE ICM 2004, IEEE ASAP 2005, IEEE IES 2006, ACM GLVLSI 2007, GRETSI 2007 EUSIPCO 2007, IEEE SIPS 2007, IEEE WCNC 2008, GRETSI 2009, IEEE ICC 2009, CHES 2009, IEEE NEWCAS (2010, 2011), CHES 2010, SOFTCOM 2011</i></p> <p>Moderator of international conferences <i>IEEE ICECS 2006, ERSA 2006, DASIP (2007, 2008, 2009, 2010), ReCoSoC (2007, 2011), CryptArchi (2007, 2008, 2009, 2010), IEEE ISVLSI 2008</i></p> <p>Invitation Keynote Speaker <i>VARY 2010, SBCCI 2011, PHYSIC 2011</i></p> <p>Round tables of international conferences <i>Summer school MDD4DRES 2006, ReCoSoC'07, IEEE ICFPT'08, ERSA 2010</i></p> <p>Summer school <i>MDD4DRES 2006, ARCHIO9, FETCH2012</i></p> <p>Guest Editor <i>EURASIP Journal on Embedded Systems, Special issue – Design and Architectures for Signal Image Processing 2009</i> <i>Book Algorithm-Architecture Matching for Signal and Image Processing Springer 2010</i> <i>Book Security trends for FPGAs: From Secured to Secure Reconfigurable Systems Springer 2011</i></p> <p>Review committee member of international journals <i>Revue scientifique francophone Traitement du signal (TS), Journal IEE Proceedings – Computers and Digital Techniques, IEEE Transactions on VLSI, IEEE Transactions on CAD, IEEE Transactions on TCSVT, IEEE Design & Test of Computers, ACM Transactions on TRET, EURASIP Journal on Embedded Systems, International Journal on Computers and Electric Engineering, International Journal of Reconfigurable Computing, The Journal of VLSI Signal Processing, Springer Journal of Real-Time Image Processing, Elsevier, Integration, the VLSI Journal, Elsevier Journal on Microprocessors and Microsystems</i></p> <p>National and international review committee member for research programs <i>Expert international NWO Computer Science Open Competition 2005 (Hollande)</i> <i>Expert international Swiss National Science Foundation (SNSF) 2009/2010/2011 (Suisse)</i> <i>Expert international PHC Germaine de Staël 2011(Suisse)</i> <i>Expert PSOC INS2I 2011</i> <i>Agence Nationale de la Recherche – Appel Architectures du futur (2006, 2007)</i> <i>Agence Nationale de la Recherche – Appel Systèmes Embarqués et Grandes Infrastructures - ARPEGE (2008, 2009)</i> <i>Agence Nationale de la Recherche - Appel Retour Post-Doctorants (2010)</i> <i>Agence Nationale de la Recherche - Appel EMERGENCE (2010)</i></p>																
International collaborations	<p>8 international collaborations with Master students, PhD students and Professor exchanges: University of Massachusetts, Amherst, USA, George Mason University, Fairfax, USA, Cambridge University, UK, Aalborg University, Denmark, Ecole Nationale d'Ingénieurs de Sfax, Sfax, Tunisia, University of de Sao Paolo, Brazil, University of Edinburgh, UK, Institut Alari, Switzerland, Karlsruhe Institute of Technology, Germany</p>																
Funding	<table border="0"> <tr> <td>FAMOUS 2013</td> <td>2009/2013, Projet ANR, Inria Lille, Lab-STICC, Inria Rhône Alpes, Le2i, Sodius</td> </tr> <tr> <td>SecReSoC 2013</td> <td>2009/2013, Projet ANR, LIRMM, Telecom ParisTech, Lhc, Lab-STICC, Netheos</td> </tr> <tr> <td>MOPCOM 2010</td> <td>2007/2010, Projet RNTL, Thales, Thomson, Ensieta, Supelec, Iriisa, LESTER, Sodius</td> </tr> <tr> <td>AETHER 2009</td> <td>2006/2009, Projet Européen IST-FET (4th call ACA / FP6)</td> </tr> <tr> <td>ICTeR 2009</td> <td>2006/2009, Projet ANR, LIRMM, Enst, List, LESTER, Netheos</td> </tr> <tr> <td>SecureNIOS 2007</td> <td>2006/2007, Projet sur fond propre, LESTER, Vspg (UMASS, USA)</td> </tr> <tr> <td>PROSYR2006</td> <td>2003/2006, CMCU, LESTER, Enis (Sfax, Tunisie)</td> </tr> <tr> <td>SANES 2005</td> <td>2004/2005, DGA ERE, LESTER, Vspg (UMASS, USA)</td> </tr> </table>	FAMOUS 2013	2009/2013, Projet ANR, Inria Lille, Lab-STICC, Inria Rhône Alpes, Le2i, Sodius	SecReSoC 2013	2009/2013, Projet ANR, LIRMM, Telecom ParisTech, Lhc, Lab-STICC, Netheos	MOPCOM 2010	2007/2010, Projet RNTL, Thales, Thomson, Ensieta, Supelec, Iriisa, LESTER, Sodius	AETHER 2009	2006/2009, Projet Européen IST-FET (4th call ACA / FP6)	ICTeR 2009	2006/2009, Projet ANR, LIRMM, Enst, List, LESTER, Netheos	SecureNIOS 2007	2006/2007, Projet sur fond propre, LESTER, Vspg (UMASS, USA)	PROSYR2006	2003/2006, CMCU, LESTER, Enis (Sfax, Tunisie)	SANES 2005	2004/2005, DGA ERE, LESTER, Vspg (UMASS, USA)
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	<p>SecureFPGA 2004 2003/2004, Projet sur fond propre, <i>LESTER, Vspg (UMASS, USA)</i></p> <p>DARSoC 2003 2002/2003, Projet sur fond propre, <i>LESTER, Vspg (UMASS, USA)</i></p> <p>A3S 2005 2003/2005, Projet RNRT, <i>Thales Communications, Softeam, Mitsubishi, LESTER</i></p> <p>POMARD 2004 2003/2004, Équipe Projet CNRS, <i>R2d2, Lien, Lirmm Le2i, Etis, List, A&S, LESTER</i></p> <p>EPICURE 2003 2001/2003, Projet RNTL, <i>I3s, LESTER, Cea/List, Thales Com., Esterel-Technologies</i></p> <p>MACGTT 2002 2000/2002, Projet CNRS, <i>I3s, Lasti, LESTER</i></p> <p>D2ASR 1999 1999, Contrat industriel, <i>LESTER, Serpe-iesm</i></p> <p>CODEF 2001 1998/2001, Contrat industriel, <i>I3s, Philips/Vlsi Technology</i></p>
Publications	<p>12 international journals (<i>ACM TODAES, ACM TECS, IEEE TCAD, IEEE TVLSI, EURASIP, ELSEVIER</i>)</p> <p>1 national journal</p> <p>5 book chapters</p> <p>2 books (Springer)</p> <p>86 publications in international conferences</p> <p>13 publications in national conferences</p> <p>1 patent</p>

Publications

Journal papers

- **Configurable Memory Security in Embedded Systems**
J. Crenne, R. Vaslin, G. Gogniat, J.-P. Diguët, R. Tessier and D. Unnikrishnan
ACM Transactions on Embedded Computer Systems (TECS), accepted September 9th 2011/to appear
- [Close-loop based self-adaptive HW/SW embedded systems: design methodology and smartcam case study](#)
J-Ph. Diguët, Y. Eustache, G. Gogniat
ACM Transactions on Embedded Computer Systems (TECS), 10, 3, Article 38 (May 2011), 28 pages.
- [A Security Approach for Off-chip Memory in embedded Microprocessor Systems](#)
R. Vaslin, G. Gogniat, J-Ph. Diguët, E. Wanderley, R. Tessier and W. Burleson
Microprocessors and Microsystems, Volume 33, Issue 1, February 2009, pages 37-45, doi: 10.1016/j.micpro.2008.08.008
Selected Papers from ReCoSoC 2007 (Reconfigurable Communication-centric Systems-on-Chip)
- [A Priori Implementation Effort Estimation for HW Design based on Independent-Path Analysis](#)
R. Abildgren, J-Ph. Diguët, P. Bomel, G. Gogniat, P. Koch, Y. Le Moullec
EURASIP Journal on Embedded Systems, Volume 2008 (2008), Article ID 280347, 12 pages, doi:10.1155/2008/280347
Special Issue on Design and Architectures for Signal and Image Processing,
- [Reconfigurable hardware for high-security/high-performance embedded systems: The SAFES perspective](#)
G. Gogniat, T. Wolf, W. Burleson, J-P. Diguët, L. Bossuet, R. Vaslin
IEEE Transactions on VLSI Systems, Vol. 16, No. 2, February 2008, pages 144-155
- [Communication-Oriented Design Space Exploration for Reconfigurable Architectures](#)
L. Bossuet, G. Gogniat, J-L. Philippe
EURASIP Journal on Embedded Systems, Volume 2007 (2007), Article ID 23496, 20 pages,
doi:10.1155/2007/23496
- [Design Space Exploration through Area and Delay Estimators for FPGAs from High Level Language](#)
S. Bilavarn, G. Gogniat, J-L. Philippe, L. Bossuet
IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, Vol. 25, No. 10, October 2006, pages 1950-1968
- [EPICURE: A partitioning and co-design framework for reconfigurable computing](#)
Jean Philippe Diguët, Guy Gogniat, Jean Luc Philippe, Yannick Le Moullec,
Sébastien Bilavarn, Christian Gamrat, Karim Ben Chehida, Michel Auguin, Xavier Fornari, Philippe Kajfasz
Journal of Microprocessors and Microsystems - Elsevier, Volume 30, Issue 6 , 4 September 2006, pages 367-387
Special Issue on FPGA's, Edited by Morris Chang and Dan Lo
- [Dynamically Configurable Security for SRAM FPGA Bitstreams](#)
L. Bossuet, G. Gogniat, W. Burleson
International Journal of Embedded Systems, IJES, From Inderscience Publishers Vol. 2, Nos. 1/2, 2006
- [Exploration de l'espace de conception des architectures reconfigurables \(in french\)](#)
Lilian Bossuet, Guy Gogniat, Jean-Luc Philippe
Revue Technique et Science Informatiques, Architecture des ordinateurs, sous la direction de Marc Daumas et Dominique Lavenier, Volume 25, n°7, pages 921 – 946, TSI, Lavoisier 2006
- [Software Radio and Dynamic Reconfiguration on a DSP/FPGA platform](#)
J-P. Delahaye, G. Gogniat, C. Roland, P. Bomel
Frequenz, Journal of Telecommunications, pages 152-159, N°58, 5-6/2004
- [A Codesign Back End Approach for Embedded System Design](#)
G. Gogniat, M. Auguin, L. Bianco, A. Pegatoquet
ACM Transactions on Design Automation of Electronic Systems, Vol. 5N. 3, july 2000
- [A Codesign experience in acoustic echo cancellation : GMDFa](#)
L. Freund, M. Israel, F. Rousseau, J. M. Bergé, M. Auguin, C. Belleudy, G. Gogniat
ACM Transactions on Design Automation of Electronic Systems, Vol. 2 N. 4, october 1997

Book Chapters

- **End-to-End Bitstreams Repository Hierarchy for FPGA Partially Reconfigurable Systems**
J. Crenne, P. Bomel, G. Gogniat, J.-P. Diguët
Algorithm-Architecture Matching for Signal and Image Processing
Series: Lecture Notes in Electrical Engineering, Vol. 73
Springer, ISBN: 978-90-481-9964-8 pp 171-194
- **Hardware Security in Embedded Systems**
L. Bossuet, G. Gogniat
Chapter 5 of Communicating Embedded Systems: Networks Applications, Francine Krief (Editor)
January 2010, Wiley-ISTE, ISBN: 978-1-84821-144-5
- [La sécurité matérielle des systèmes embarqués \(in french\)](#)
L. Bossuet, G. Gogniat
Chapter 5 of Traité 12C, Systèmes Embarqués Communicants, Edited by F. Krief
Hermes edition - Lavoisier, 2008

- [Schedulability Analysis and MDD, From MDD Concepts to Experiments and Illustrations](#)
S. Rouxel, G. Gogniat, J-P. Diguët, J-L. Philippe and C. Moy
Chapter 7. Edited by: J-P. Babau, J. Champeau, S. Gérard
International Scientific and Technical Encyclopedia, September 2006, pages 111 – 130

Books

- [Algorithm-Architecture Matching for Signal and Image Processing](#)
Best papers from Design and Architectures for Signal and Image Processing 2007 & 2008 & 2009
Lecture Notes in Electrical Engineering, Vol. 73
Gogniat, G.; Milojevic, D.; Morawiec, A.; Erdogan, A. (Eds.)
Springer, 1st Edition., 2011, XI, 296 p.
- [Security Trends for FPGAS](#)
From Secured to Secure Reconfigurable Systems
Badrignans, B.; Danger, J.L.; Fischer, V.; Gogniat, G.; Torres, L. (Eds.)
Springer, 1st Edition., 2011, XX, 252 p.

International Conference papers

- **Efficient Key-Dependent Message Authentication in Reconfigurable Hardware**
J. Crenne, P. Cotret, G. Gogniat, R. Tessier, and J.-P. Diguët
in the Proceedings of the International Conference on Field-Programmable Technology (FPT'11), December 12-14, 2011, New Delhi, India
- **Dynamic NoC-Based Architecture for MPSoC Security Implementation**
Johanna Sepúlveda, Guy Gogniat, Ricardo Pires, Wang Jiang Chau, Marius Strum
in the Proceedings of the Symposium on Integrated Circuits and Systems Design (SBCCI'11), August 30th to September 2nd, 2011, João Pessoa, Brazil
- **Asymmetric Cache Coherency: Improving Multicore Performance for Non-uniform Workloads**
John Shield, Jean-Philippe Diguët and Guy Gogniat
6th International Workshop on Reconfigurable Communication-centric Systems-on-Chip (ReCoSoC'11), June 20 – 22, 2011, Montpellier, France
- [A multi-objective approach for multi-application NoC mapping](#)
Sepúlveda, J.; Strum, M.; Wang Jiang Chau; Gogniat, G.;
IEEE Second Latin American Symposium on Circuits and Systems (LASCAS), 2011
- [Dynamic applications on reconfigurable systems: From UML model design to FPGAs implementation](#)
Vidal, J.; de Lamotte, F.; Gogniat, G.; Diguët, J.-P.; Guillet, S.;
Design, Automation & Test in Europe Conference & Exhibition (DATE), 2011
- [Distributed security for communications and memories in a multiprocessor architecture](#)
P. Cotret, J. Crenne, G. Gogniat, J.P. Diguët, L. Gaspar, G. Duc
RAW'11: IEEE 18th International Conference on Reconfigurable Architectures Workshop, Anchorage, USA, 16-17 May 2011
- [Design and Implementation of a Multi-Core Crypto-Processor for Software Defined Radios](#)
Michael Grand, Lilian Bossuet, Bertrand Le Gal, Guy Gogniat, Dominique Dallet
ARC 2011: 29-40
- [A Reconfigurable Multi-core Cryptoprocessor for Multi-Channel Communication Systems](#)
Michael Grand, Lilian Bossuet, Guy Gogniat, Bertrand Le Gal, Jean-Philippe Delahaye and Dominique Dallet
RAW'11: IEEE 18th International Conference on Reconfigurable Architectures Workshop, Anchorage, USA, 16-17 May 2011
- [Modeling and Formal Control of Partial Dynamic Reconfiguration](#)
Sébastien Guillet, Florent de Lamotte, Éric Rutten, Guy Gogniat, Jean-Philippe Diguët
ReConFig 2010: 31-36
- [XPSoC: A reconfigurable solution for multimedia contents protection](#)
Lin Feng Ye, Jean-Philippe Diguët, Guy Gogniat
HPCS 2010: 504-508
- [A Multi-Core AES Cryptoprocessor for Multi-Channel SDR](#)
Michael Grand, Lilian Bossuet, Bertrand Le Gal, Dominique Dallet, Guy Gogniat
Military Communication and Information Systems Conference, MCC 2010, Wrocław : Poland (2010)
- [Rapid Application Development on Multi-processor Reconfigurable Systems](#)
Lin Feng Ye, Jean-Philippe Diguët, Guy Gogniat
FPL 2010: 285-290
- [Predictability of inter-component latency in a software communications architecture operating environment](#)
Abgrall, Gael; Le Roy, Frederic; Diguët, Jean-Philippe; Gogniat, Guy; Delahaye, Jean-Philippe
2010 IEEE International Symposium on Parallel & Distributed Processing, Workshops and Phd Forum (IPDPSW), 2010, Page(s): 1 - 8
- **Latency estimation due to middleware used in Software Defined Radio Platform**
G. Abgrall, F. Le Roy, J-P. Diguët, G. Gogniat, J-P. Delahaye
6th Workshop on Software Radio, Karlsruhe, Germany, March 3-4 2010.

- [**UML design for dynamically reconfigurable multiprocessor embedded systems**](#)
Vidal, J.; de Lamotte, F.; Gogniat, G.; Diguët, J.-P.; Soulard, P.
Design, Automation & Test in Europe Conference & Exhibition (DATE), 2010, Page(s): 1195 - 1200
- [**Self-reconfigurable embedded systems: from modeling to implementation**](#)
G. Gogniat, J. Vidal, L. Ye, J. Crenne, S. Guillet, F. de Lamotte, J.-P. Diguët, P. Bomel
Engineering of Reconfigurable Systems and Algorithms (ERSA), July 13-16, 2010, Las Vegas, Nevada, USA
- [**Networked Self-adaptive Systems: An Opportunity for Configuring in the Large**](#)
J.-P. Diguët, L. Ye, Y. Eustache, J. Crenne, P. Bomel, G. Gogniat, J. Vidal, F. de Lamotte
Engineering of Reconfigurable Systems and Algorithms (ERSA), July 13-16, 2009, Las Vegas, Nevada, USA
- [**IP reuse in an MDA MPSoPC co-design approach**](#)
Vidal, J.; de Lamotte, F.; Gogniat, G.; Diguët, J.-P.; Soulard, P.
International Conference on Microelectronics (ICM), 2009, Page(s): 256 - 259
- [**Reconfigurable Crypto Sub System for the Software Communication Architecture**](#)
M. Grand, L. Bossuet, B. Legal, D. Dallet, G. Gogniat
MILCOM 2009, October 18–21, 2009, Boston, MA USA
- [**Modeling of Reconfigurable MPSoCs for On-Demand Computing**](#)
L. Ye, J.-P. Diguët, G. Gogniat
XXII Colloque GRETSI, September 2009
- [**Configuration server for self-adaptive architectures**](#)
L. Ye, J.-P. Diguët, G. Gogniat
Conference Design and Architectures for Signal and Image Processing, 2009. DASIP'09, September 2009
- [**UDP partial bitstreams diffusion through WLAN**](#)
J. Crenne, P. Bomel, G. Gogniat, and J.-P. Diguët
Conference Design and Architectures for Signal and Image Processing, 2009. DASIP'09, September 2009
- [**A co-design approach for embedded system modeling and code generation with UML and MARTE**](#)
J. Vidal, F. De Lamotte, G. Gogniat, P. Soulard
Design, Automation & Test in Europe (DATE 2009), 20-24 April, Nice, France, 2009
- [**Ultra-Fast Downloading of Partial Bitstreams Through Ethernet**](#)
P. Bomel, J. Crenne, L. Ye, J.-Ph. Diguët, G. Gogniat
International Conference on Architecture of Computing Systems, 10-13 March, Delft, Netherlands, 2009
- [**Memory Security Management for Reconfigurable embedded Systems**](#)
R. Vaslin, G. Gogniat, J.-Ph. Diguët, R. Tessier, D. Unnikrishnan, K. Gaj
International Conference on Field-Programmable Technology 2008 (ICFPT'08), Taipei, Taiwan, December 7th - 10th, 2008.
- [**A Method for A Priori Implementation Effort Estimation for Hardware Design**](#)
R. Abildgren, J.-Ph. Diguët, P. Bomel, G. Gogniat, P. Koch, Y. Le Moullec
Proc. of Intl. Consortium for Educational Development (ICED 2008), Penang, Malaisie, décembre 2008
- [**Bitstreams Repository Hierarchy for FPGA Partially Reconfigurable Systems**](#)
P. Bomel, G. Gogniat, J.-P. Diguët, J. Crenne
Proc. of 7th International Symposium on Parallel and Distributed Computing (ISPDC'2008) Cracovie, Pologne, 1-5 juillet 2008.
- [**System level design space exploration for multiprocessor system on chip**](#)
I. Maalej, G. Gogniat, J.-L. Philippe, M. Abid
ISVLSI 2008 - IEEE Computer Society Annual Symposium on VLSI - 2008, April 7-9, Montpellier, France
- [**A Networked, Lightweight and Partially Reconfigurable Platform**](#)
P. Bomel, G. Gogniat and J.-P. Diguët
Proc. of 4th Intl. Workshop on Applied Reconfigurable Computing (ARC'2008) Imperial College, Londres, Royaume Uni, 26-28 mars 2008 LNCS 4943, Reconfigurable Computing : Architectures, Tools and applications ISSN 0302-9743, ISBN-10 3-540-78609-0 Springer Berlin Heidelberg New-York
- [**Hardware implementation of a multi-mode hash architecture for MD5, SHA-1 and SHA-2**](#)
S. Ducloyer, R. Vaslin, G. Gogniat, E. Wanderley
Workshop on Design and Architectures for Signal and Image Processing, November 27-29, 2007, Grenoble, France
- [**Operating Environment online Metrics for Application Architecture Matching**](#)
M. El Khodary, J.-Ph. Diguët, G. Gogniat
25th IEEE Norchip Conference, 19-20 Nov. 2007, Aalborg, Denmark
- [**A Code Compression Method to Cope with Security Hardware Overheads**](#)
E. Wanderley, R. Vaslin, G. Gogniat, J.-P. Diguët
19th IEEE International Symposium on Computer Architecture and High Performance Computing, October 24-27, 2007, Gramado, RS, Brazil
- [**High Efficiency Protection Solution for Off-Chip Memory in Embedded Systems**](#)
R. Vaslin, G. Gogniat, J.-P. Diguët, R. Tessier, W. Burseson
The International Conference on Engineering of Reconfigurable Systems and Algorithms, June 25-28, 2007, Las Vegas, Nevada, USA
- [**A Code Compression Method With Confidentiality and Integrity Checking**](#)
E. Wanderley, G. Gogniat, J.-P. Diguët
The 2007 International Conference on Embedded Systems and Applications, June 25-28, 2007, Las Vegas, Nevada, USA
- [**IBC-El: An Instruction Based Compression method with Encryption and Integrity Checking**](#)
E. Wanderley, R. Elbaz, L. Torres, G. Sassatelli, R. Vaslin, G. Gogniat, J.-P. Diguët

3rd International Workshop on Reconfigurable Communication Centric System-on-Chips (ReCoSoC'07),
18th-20th June 2007, Montpellier, France

- [Low latency solution for confidentiality and integrity checking in embedded systems with off-chip memory](#)
R. Vaslin, G. Gogniat, E. Wanderley, R. Tessier, W. Burlleson
3rd International Workshop on Reconfigurable Communication Centric System-on-Chips (ReCoSoC'07),
18th-20th June 2007, Montpellier, France
- [The Allele Search Lab to Improve Heterogeneous Reconfigurable Platform Design Skills](#)
Y. Eustache, J-P. Diguët, G. Gogniat
The 2nd International Workshop on Reconfigurable Computing Education, May 12, 2007, Porto Allegre, Brasil
- [NOC-centric security of reconfigurable SoC](#)
J-P. Diguët, G. Gogniat, S. Evain, R. Vaslin, E. Juin
The 1st ACM/IEEE International Symposium on Networks-on-Chip,
May 7-9, 2007, Princeton University, New Jersey, USA
- [Bus Decryption Overhead Minimization with Code Compression](#)
E. Wanderley, G. Gogniat, J-P. Diguët
The 3rd IEEE Southern Conference on Programmable Logic,
February 26-28, 2007, Mar del Plata, Argentina
- **Genetic algorithm for high level analysis and architecture exploration**
I. Maalej, G. Gogniat, J-L. Philippe, M. Abid
IP Based Design 2006 Workshop, December 2006, Grenoble, France
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