An Evolutive Approach for Designing Thermal and Performance-Aware Heterogeneous 3D-NoCs

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***Abstract*—Three dimensional Multiprocessor System-on-Chip (3D-MPSoC) adoption. It is characterized by the integration of a large amount of hardware components on a single multilayer chip. However, heating is one of the major pitfalls of the 3D-MPSoCs. Three dimensional Network-on-Chip (3D-NoC) is used as the communication structure of 3D-MPSoCs. Its main role in system operation and performance makes the optimal 3D-NoC design a critical task. Final 3D-NoC configuration must fulfill all the application requirements and heating constraints of the system. Topology and mapping are some of the most critical parameters in 3D-NoC design, strongly influencing the 3D-MPSoC performance and cost. 3D-NoC topology and mapping has been solved for single application systems on homogeneous 3D-NoCs using single and multi-objective optimization algorithms. In this paper we use a multi-objective immune algorithm (MIA), to solve the multi-application 3D-NoC topology and mapping problems. Latency and power consumption are adopted as the target multi-objective functions constrained by the heating function. Our strategy has been applied on 8 3D-MPSoC benchmarks. Their final 3D-NoC configurations have up to 73% power and 42% latency enhancement when compared to previous reported results.**

I. INTRODUCTION

Three-dimension Multiprocessor System-on-Chip (3D-MPSoC) promises to overcome such challenges by stacking multiple programmable processor cores, specialized memories and other intellectual property (IP) components on a single chip. 3D-MPSoC brings as its major advantage the capability of supporting many applications on a single chip. Each application is characterized by a set of performance requirements. Therefore, there is not a single, but a set of performance requirements that must be satisfied. However, vertical integration of layers exacerbates the thermal problems. Heating is one of the major pitfalls of the 3D-MPSoCs. They are prone to hotspots due the overloading of tasks execution on some 3D-MPSoCs areas. Managing heterogeneous workloads to optimize performance and temperature is challenging.

In order to support the 3D-MPSoC high communication requirements three dimension Network-on-Chip (3D-NoC) is employed [4-6]. 3D-NoC is an integrated network that uses routers and links to allow the vertical and horizontal communication among the IPs. Vertical links communicate different dies by mean of Through-Silicon-Vias (TSVs). TSVs are conductive nails which extend out the back-side of a thinned-down die [5]. A set of TSVs are called *pillars*. Compared to traditional wire bonds, TSVs are short and low-capacity interconnection, able to operate at high frequencies. However, fabrication constraints turn TSVs difficult to build and area costly (due to the pitch between TSVs). 3D-NoCs can be homogeneous or heterogeneous according to the way the pillars are allocated. In a homogeneous 3D-NoC, each router has a *pillar,* otherwise, they are called heterogeneous. Homogeneous 3D-NoC is a regular topology which provides multiple paths for the inter-layer communication. However, the cost of a pillar is high. Heterogeneous 3D-NoC can reduce the overall system cost significantly [5]. Fig. 1 shows a homogeneous 3D-MPSoC that integrates 27 IPs in three layers through a 3D-NoC.

Among all the 3D-NoC configuration parameters, *topology* and *mapping* have a great impact on the cost and on the performance of the 3D-MPSoC [5]. Topology and mapping are quadratic assignment problems that are known to be NP-hard [2]. The search space of the problem increases in a factorial manner with the system size [1,2]. This paper addresses the 3D-NoC *topology and mapping problems*. *Topology* defines the number and allocation of the 3D-NoC vertical pillars. *Mapping* deals with the association of each IP cores to a network router. The final configuration must fulfill all applications requirements and optimize some performance metrics under heating constraints [1].

The best 3D-NoC solutions have been obtained using a multi-objective strategy [5]. As a result, the designer obtains a set of best mapping alternatives (*Pareto optimal set- POS, non-dominated solutions*) featuring different trade-offs among the performance indexes [2]. Pareto dominance is used to compare and rank the mapping solutions. A mapping belongs to the *Pareto optimal set* if there is no other mapping that can improve at least one of the objectives without degrading any other objective (*non-dominance*) [7].

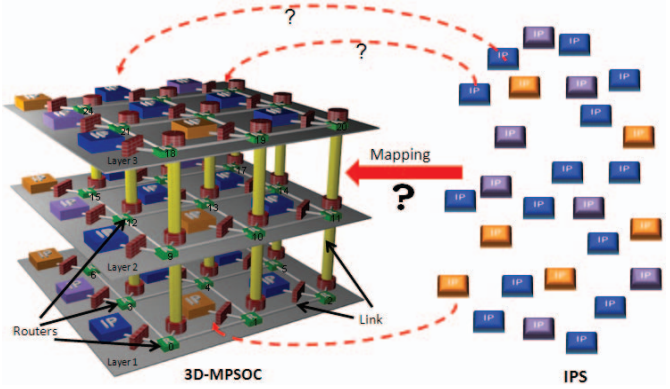

Figure 1. Mapping problem for 3D-NoC-based 3D-MPSoC

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Only [9], has proposed a multi-objective 3D-NoC mapping based on a rank-based genetic algorithm (RMGA) with the purpose of reducing the latency under congestion and the latency under non-congestion (agreeing objectives). However, heating issues of the 3D-MPSoC are not taken into account.

In this work we propose MIA, a Multi-objective adaptive Immune Algorithm to solve the multi-application 3D-NoC topology and mapping problems with the purpose of reducing the latency and power constraints under heating constraints. MIA explores the topology and mapping space producing a set of best 3D-NoC alternatives. We compared our solution with a modified version that we implemented for the RMGA (3D-RMGA). The Pareto optimal set of the two algorithms were then evaluated and compared using a NoC-based TLM *(SystemC)* simulation environment.

For the best of our knowledge, this work presents four novelties: i) the use of a multi-objective immune algorithm to solve the 3D-NoC topology and mapping problems under contrasting objectives (power and latency); ii) the solution of the 3D-NoC topology and mapping problems for multi-application systems; iii) the consideration of heating constraints; and iv) the static (analytical model) and dynamic (simulation) evaluation of the solutions.

The remaining text is divided into seven sections. Section 2 presents an overview of the previous 3D-NoC mapping works. Section 3 presents the topology and mapping problems. Section 4 describes MIA mapping algorithm. Section 5 presents the analytical models employed to evaluate the 3D-NoC alternatives. Section 6 shows our experimental results. Finally we present our conclusions in Section 7.

II. Related Works

As 3D-MPSoC is a new technology, the 3D-NoC mapping has been only recently explored [3,5]. The purpose of these previous works is to find a 3D-NoC configuration that satisfies the requirements of a single application 3D-MPSoC. Multiple application systems have not been addressed before. All previous [3,5] use an application characterization graph (APCG) that describes the communication requirements. In [5], the authors present a heuristic algorithm that selects the first 3D-NoC configuration that satisfies the single application 3D-MPSoC latency requirement. The work of [3] employs a multi-objective rank-based genetic algorithm (RMGA) to find the 3D-NoC mapping that optimizes the latency under congestion and the latency under non-congestion (agreeing objectives). It codifies the different mapping alternatives in chromosomes. Elitism, crossover and mutation operators are used in order to explore the mapping space (creating new mapping alternatives). The mapping alternatives are evaluated through an analytical model (static model). Despite their good results, these strategies present some difficulties: i) they support only the mapping for single application systems, ignoring the capacity of 3D-MPSoC to support different applications during the execution time; ii) the strong elitism may incur high selection pressure, thereby leading to premature convergence. This lack of diversity (it progresses around the best solution) may result in suboptimal solutions; iv) all previous approaches use only a static model to evaluate and select a mapping alternative, ignoring the strong impact on the dynamic behavior of the traffic over the 3D-NoC performance. This characteristic can generate suboptimal solutions; and v) none of these works takes into account the heating constraints of the 3D-MPSoC. Therefore the mapping solutions may be prohibitive and cause serious damage to the system. For the best of our knowledge our work is the first attempt that addresses the multi-application 3D-NoC topology and mapping under heating constrained systems while optimizing multiple and contrasting performance indexes.

III. Problem Description

A. 3D-NoC topology

3D-NoCs are used as the communication structure of 3D-MPSoCs. They use a set of routers and links to interconnect IPs, which in turn are used to execute the tasks of different applications at the 3D-MPSoC. A 3D-NoC router defines the path that the information must follow through the network from the initiator to the destination IP.

Topology is defined as the particular interconnection used among the routers of the 3D-NoC. Formally, 3D-NoC topology, 3D-*TP,* is defined by a digraph *T(R,U)*, where each vertex $r \in R$ represents a router integrated in the 3D-NoC and each edge $u \in U$ corresponds to a communication link between two routers. Each *r* belongs to a layer L of the 3D-MPSoC and is constrained by T_{max}, the maximum temperature allowed at *r*. It depends on technological factors, on the layer of the 3D-MPSoC and on the power consumed by *r*.

3D-NoC topology can be divided into 2 categories: i) horizontal, which defines the connection among the routers at the same layer; and ii) vertical, which define the number and allocation of the pillars that links two routers placed at different layers.

Electrical and geometrical concerns made the homogeneous stacked mesh-based 3D-NoC the most popular topology [4-6]. See Fig. 1. It is characterized by a mesh-based horizontal topology. Moreover, it uses a six-port router to communicate all the IPs at the 3D-MPSoC. Each router is connected to its neighboring routers via two unidirectional links. However, the vertical topology integrates a high number of pillars. Therefore, the high number of TSVs turns the stacked topology in a costly solution in terms of area and power [5]. However, the reduction of number of *pillars* may generate hot spots in the 3D-MPSoC due to the concentration of traffic around them in order to perform vertical communication. The goal is to find the topology 3D-TP that minimizes the number of pillars and fulfills the requirements of the applications. The minimum number of *pillars* between two consecutive layers is 1.

B. 3D-NoC mapping

After the topology definition, the next step of the 3D-NoC design process is to connect each particular IP to a router. It chooses a location in the 3D-NoC structure for each IP. This process is called 3D-NoC mapping. It has a huge impact on the network performance [5]. The initiator/destination

locations in the 3D-MPSoCs define the traffic over the network. The closer they are, the smaller the probability of congestion. However, if several power hungry IPs or high traffic nodes are located in a same area of the 3D-MPSoC, hot spots can be created. This may cause malfunction or infeasibility of the system.

Formally, the mapping problem can be described as follows. Each application A is defined by an Application Communication Graph (APCG). The *APCG(V,E)* is a digraph, where each vertex $v \in V$ represents an IP integrated in the 3D-MPSoC and each edge $e \in E$ defines the communication between a pair of IPs. It has two attributes: i) the required latency; and ii) the amount of data.

The goal is to find the mapping M that allocates all the IPs to 3D-TP, such that it fulfills the required latency of all the applications and the power restriction of the 3D-MPSoC.

IV. MIA

A. MIA General Description

An immune system protects the organism by producing antibodies capable of identifying attackers (antigens). It constantly monitors the defense process through the evaluation of the *affinity* and *avidity*. They quantify the match between antigen-antibody pairs (for recognition) and between a single antibody and the whole antibody population (for diversity). The survival of a specific antibody depends on these values. The immune system integrates a wide set of mechanisms: pattern recognition (affinity), clonal selection (cloning the antibodies that best match the antigen), clonal suppression (killing the worst antibodies), mutation (modifying a set of antibodies), affinity maturation (creating a new set of antibodies), learning and memory (storing the successful antibodies). Immune algorithms (IA) have been successfully used in several optimization problems [7]. MIA uses an immune algorithm to solve the vertical topology and mapping problems. Table 1 shows the metaphors employed by MIA.

To solve these problems, MIA requires i) the set of APCGs of the applications that are going to be executed in the 3D-MPSoC; ii) heating constraints; and iii) the number of layers. Our work assumes that 3D-NoC is used to connect a set of IP components of the same size. Floorplanning considerations are part of future works. MIA assumes that each IP is linked to a router and that the 3D-NoC implements a mesh-based horizontal topology. MIA is composed of 7 phases

Phase 1: MIA generates the Worst-Case APCG (W-APCG), as a result of the combination of the APCGs of the applications executed on the 3D-MPSoC. W-APCG includes all 3D-MPSoC IP cores. For the communication flow between every pair of IP cores, the tightest communication requirements across all the applications are selected as the requirements of the W-APCG. Thus the design constraints of all the individual applications are subsumed in the W-APCG and any 3D-NoC that satisfies the constraints in the W-APCG will satisfy the constraints of each individual application.

Phase 2: MIA generates the initial set of 3D-NoC alternatives. It is composed of M random generated and designer suggested 3D-NoC topology and mapping alternatives. Each alternative consists of two segments: i) Mapping alternative: links IP to a router; and ii) Vertical topology: expresses the number and location of the pillars. 3D-NoC alternatives (antibodies) are encoded by means of real representation. Fig 2 shows an example of a 3-layer 3D-NoC alternative. Router 4 is linked to the IP 5 and there are two pillars between routers 9-0, 2-11.

Phase 3: Evaluation of the *objective functions (fitness),* power consumption and latency of all the 3D-NoC alternatives. Evaluate heating and verify if it meets the constraints. See Section V.

Phase 4: Ranking of 3D-NoC alternatives according to the *dominance value* of the objective functions results. A 3D-NoC alternative is dominated by the solutions with lower *objective function* values [7]. Each m 3D-NoC is assigned a fitness value $r(m,i)$ based on its rank $d(m,i)$ at i iteration (1).

$$r(m,i) = 1 + d(m,i) \quad (1)$$

Phase 5: Refining the *POS*. The N non-dominated 3D-NoC alternatives ($r(m,i)=1$) are copied (cloned) and stored in memory (*POS*). The non-dominance characteristic of all the stored 3D-NoC solutions is verified. The new non-dominated alternatives are kept as part of the set of solutions. The remaining ones are erased from memory.

Phase 6: Ranking the remaining *(M-N)* dominated 3D-NoC alternatives ($r(m,i)\neq 1$) according to two parameters: 1) the objective function; and the 2) avidity (normalized sum of euclidean distances between every solution pair). The purpose is to identify and penalize 3D-NoC solutions in densely populated areas. The position in the ranking determines the selection probability for each 3D-NoC alternative.

Phase 7: Generating M new 3D-NoC alternatives. Two operators were employed: crossover and mutation. The crossover operator (Fig 4) creates a new 3D-NoC (M3) from the combination of two different 3D-NoCs (M1, M2). The mutation changes one or multiple genes inside the antibody according to the mutation rate. Then since phase 3, all the phases are executed. MIA stops when no more significant improvement can be expected.

Table 1. Immune system metaphors.

Immune system feature	*MIA*
Antigen	Worst case Application characterization graphs (W-APCG)
Antibody	3D-NoC alternative *M*
Pattern recognition	Multi-objective quantification
Clonal selection	Top 3D-NoC alternatives selection
Clonal suppression	3D-NoC alternatives elimination
Mutation	3D-NoC alternatives modification
Maturation	3D-NoC alternatives creation
Learning and memory	3D-NoC solutions

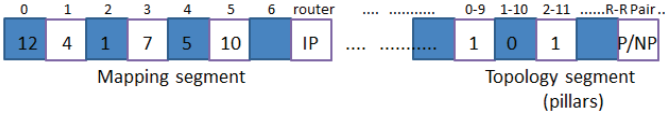

Figure 2. 3D-NoC alternative (antibodies) representation.

B. Setting MIA control parameters

The performance of MIA depends on many factors, such as selection schemes and control parameters. The goal of MIA is to converge to the optimal 3D-NoC in as few generations (iterations) as possible. Mutation rate is considered one of the most sensitive parameters for the immune algorithms [7]. It increases the diversity in the population, so as to prevent getting stuck at a local optimal value during the optimization search [10]. According to the mutation rate μ_r, the 3D-NoC alternatives are modified. In the first segment one or more pairs of router-IP; and in the second, the number and allocation of pillars. MIA uses an adaptive mutation rate, which varies according to the fitness value of the 3D-NoC alternatives. μ_r is increased when the population is getting stuck at a local optimum. μ_r is decreased when the population is spread along the solution space. μ_r varies in the range of [0.02, 0.1] and it is given by (2).

$$\mu_{ri} = k.\frac{D_{fmap}}{D_{fave}} \tag{2}$$

This range was selected after tests performed for different static mutation rates (See Section VIB). To determine whether MIA is converging/diverging, two distances are used: i) D_{fave}, distance between the average fitness (f_{ave}) and the maximum fitness (f_{max}); and ii) D_{fmap}, distance between each 3D-NoC alternative fitness (f_{map}) and the maximum fitness (f_{max}). Note that μ_r has a lower value for high fitness 3D-NoCs and higher value for lower fitness 3D-NoCs. The high fitness 3D-NoCs aid the convergence of MIA, while low fitness 3D-NoCs prevent that MIA gets stuck at a local optimum.

V. ANALYTICAL MODEL

MIA uses an analytical 3D-NoC model built from the queueing theory. In this approach, the 3D-NoC routers are represented as a collection of *service centers,* composed of queues and servers, whose purpose is to attend the communication of packets.

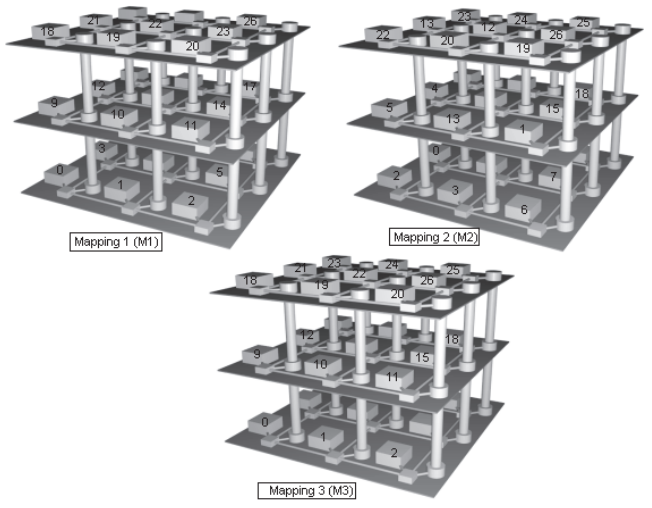

Figure 3. M3: Crossover of M1 and M2 3D-NoC alternatives.

A. Latency

The latency of the router L_r is defined as the average time elapsed from a packet arrival to a router input port to its departure from one of its outputs. L_r is given by (3), where t_a is the arbitration delay (which controls the packet traffic inside the router) and t_s is the switching time.

$$L_r = \frac{\sum t_a + t_s}{\#bits} \tag{3}$$

t_a is given by (4) [5], where p is the number of ports of the router and τ corresponds to the delay of the minimum sized inverter for the target technology. t_s is a constant which value depends on technological parameters.

$$t_a = \left[21\left(\frac{1}{4}\right)\log_2 p + 14\left(\frac{1}{12}\right)\tau + 9 \right] \tag{4}$$

3D-NoC is modeled as an open network of *service centers*, that is, data come from sources to be commuted by the 3D-NoC routers until being delivered to a specific sink, the target of the communication. 3D-NoC latency L_{3DNoC} is given by (5). It is determined by four components: i) the time t_{acc} to access the 3D-NoC and insert the data from the IP initiator to its router; ii) the router latency L_r, spent by the intermediate h routers from s source to d destination ; iii) the delay due to the links; and iv) the time t_{lea} required to leave the 3D-NoC.

$$L_{3DNoC} = \frac{\sum t_{acc} + (h_{s,d} - 1)L_r + t_L + t_{lea}}{\#bits} \tag{5}$$

Where t_L is given by (6). It includes t_v, the delay caused by V vertical links; and t_h due to the H horizontal links. Horizontal and vertical links have different electric characteristics that generate different delays.

$$t_L = \sum_V t_v + \sum_H t_h \tag{6}$$

B. Power

P_{3DNoC}, the 3D-NoC power given by (7), is determined by P_R and P_L, the power consumed in the routers and links respectively. P_R and P_L are proportional to the *router utilization rate* and *channel utilization rate*. P_v, and P_h, represents the power consumed at the V vertical and H horizontal links.

$$P_{3DNoC} = \frac{\sum_R (h_{s,d} + 1)P_r + \sum_V P_v + \sum_H P_h}{\#bits} \tag{7}$$

C. Thermal Function

The heating at the location β of the 3D-NoC is defined by the thermal function T_β, given by (8). It is primarily determined by the power at this point as well as by its location within the 3D-MPSoC [4,5].

$$T_\beta = R_{eff}.A.(V_\beta{}^2.F_i) \tag{8}$$

Where R_{eff} is the effective thermal resistance. It is a function of technological parameter, the layer of the 3D-MPSoC and the location in the layer. A represents the amount of data commuted by the router at β, V_β and F are the voltage and frequency of the layer of the 3D-MPSoC.

VI. Experimental Work

A. Experimental Setup

MIA was tested and compared with the multi-objective rank-based genetic algorithm (3D-RMGA) [3]. We implemented both algorithms in C++ and both were executed on a Pentium IV – 1,73 GHz personal computer. For comparison purposes, the two algorithms use the same analytical models described at the Section V. The objective functions are given by (5) and (7) respectively. As heating constraints were used the values presented at [5]. In order to solve the 3D-NoC topology and mapping problem, the experimental work is divided into 3 sections: i) tuning of MIA parameters; ii) execution of the tuned MIA in order to find the set of best 3D-NoC alternatives to each test; and iii) simulation of POS in SystemC-TLM.

All the tests were performed on a 3-layer 3D-MPSoC, wormhole mesh-based horizontal topology 3D-NoC, using a XYZ routing algorithm, 16 bits sized buffers and a round-robin arbitration technique. The multi-objective algorithms were used to solve the topology and mapping problem of 8 multi-application benchmarks. Table 2 shows the characteristics of the experiments. The APCG values of each benchmark were randomly selected. Benchmarks T1-T4 combine different well-known embedded communication patterns [8]. Benchmarks T5-T8 are part of MiBench tool suite. Each benchmark is composed of a set of applications targeting a specific area of the embedded market: automotive, consumer devices and security. The column *routers* define the number of routers per layer of the 3D-MPSoC.

B. Tuning of the MIA parameters

The purpose of the first set of experiments is to find the MIA configuration parameters which speed up its convergence. We measure the sensibility of MIA over the mutation rate μ_r in terms of the number of generations required to find the POS. Each point of the Fig 4 was evaluated by taking the average of 100 independent runs of MIA. μ_r was varied from 0.01 to 1. The population size was fixed to 200. The results show the huge impact of μ_r over the performance of MIA. Each benchmark presents a different optimal mutation rate μ_r. We observe that the best performances of MIA are achieved for μ_r values in the interval [0.02, 0.1]. Moreover, the results of the Fig 4, suggest that an adaptive mutation rate μ_r inside that interval may result in higher improvement. In order to probe this hypothesis, a second experiment was conducted. We evaluate and compare the effect on the performance of MIA for a static (μ_r= *0.03*) and dynamic mutation rates. The dynamic mutation rate is explained at Section IV. The results are showed at Fig 5. The adaptive mutation rate approach always outperforms the static approach and enhances the MIA performance up to 84%. Table 3 shows the configuration parameters of MIA, defined after the first set of experiments.

Table 2. Characteristics of the experimental work

Benchmark	#IP's	Routers	#APCGs	Type of traffic
T1	12	4/4/4	5	Uniform
T2	27	9/9/9	4	Hot spot
T3	48	16/16/16	5	Transpose
T4	75	25/25/25	3	Uniform
T5	108	36/36/36	3	Uniform
T6	147	49/49/49	8	Uniform
T7	192	64/64/64	5	Uniform
T8	243	81/81/81	8	Uniform

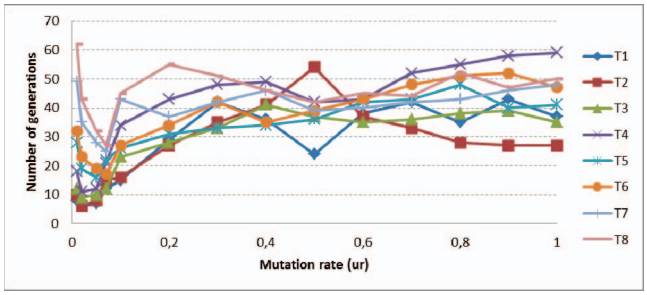

Figure 4. Impact of mutation rate over MIA.

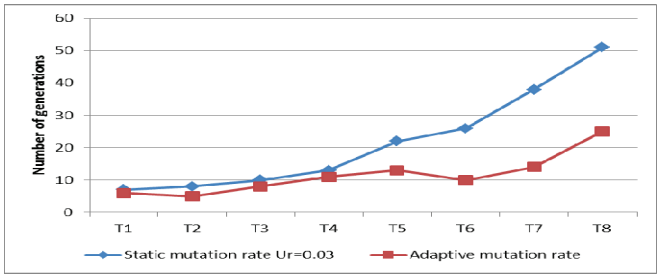

Figure 5. Static versus dynamic mutation rate.

C. Quality of the 3D-NoC solutions

Figures 6 and 7 show the analytical L_{3DNOC} and P_{3DNOC} results for the best latency-3D-NoC of the POS set of MIA and 3D-RMGA. It shows also the variance among all the POS. Figures 8 and 9 show the TLM-based simulation results for the 3DNoC latency and 3DNoC latency respectively of the POS of the two algorithms. The comparisons among these results show the fidelity of the prediction of the analytical model. However, there is a lack of precision. This fact appears from the difficulty of the analytical (static) model to represent the dynamic behavior of the 3D-MPSoC.

Table 3. MIA parameters

Parameter	*Value*
Initial population M (phase 2)	100 – 200
Latency objective function	L_{3DNoC}
Power objective function	P_{3DNoC}
Heating function	T_β
Dynamic mutation rate (phase5)	[0.02, 0.05]
Crossover (phase7)	40%
Stop criterion	0.1

Therefore, in order to solve the topology and mapping problems is important to analyze both, the static and dynamic behavior of the 3D-MPSoC. All the experiments show that it is possible to obtain high performance heterogeneous 3D-NoC. MIA was able to find better solutions that 3D-RMGA. This is due to the diversity characteristic of MIA. The final 3D-NoC heterogeneous configurations found by MIA enhance up to 73% the power and 42% the latency when compared to the 3D-RMGA results. Although the latency of the heterogeneous increase up to 12% compared with the homogeneous approach, the cost in terms of area (expressed as number of *pillars*) and power decreases up to 45% and 38% respectively. Table 4 summarizes the results for the heterogeneous 3D-NoC when compared to the homogeneous solutions.

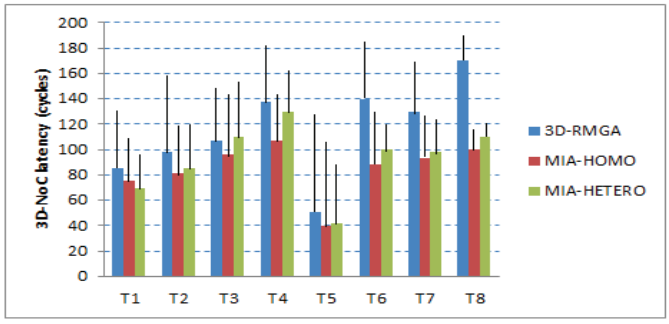

Figure 6. 3D-NoC latency static evaluation results.

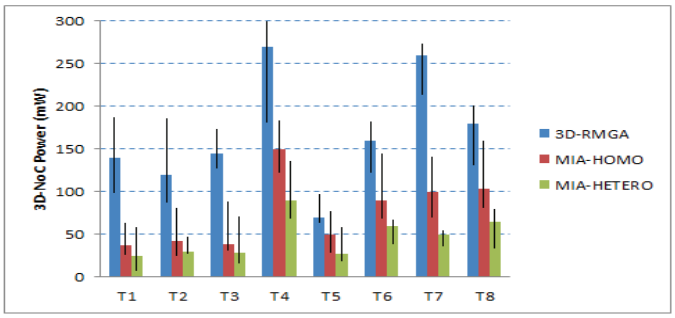

Figure 7. 3D-NoC power static evaluation results.

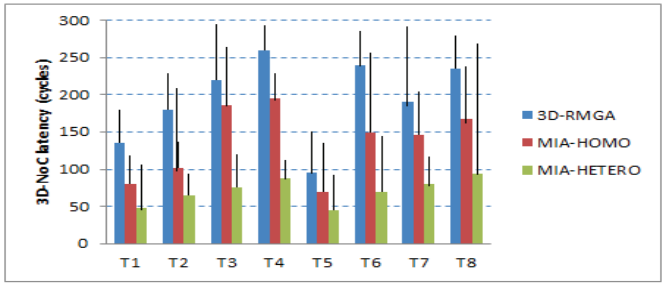

Figure 8. 3D-NoC latency dynamic evaluation results.

Table 4. Improvements of heterogeneous 3D-NoC

Configuration	*Latency*	*Power*	*Area*
MIA-HETERO	-12%	38%	65%

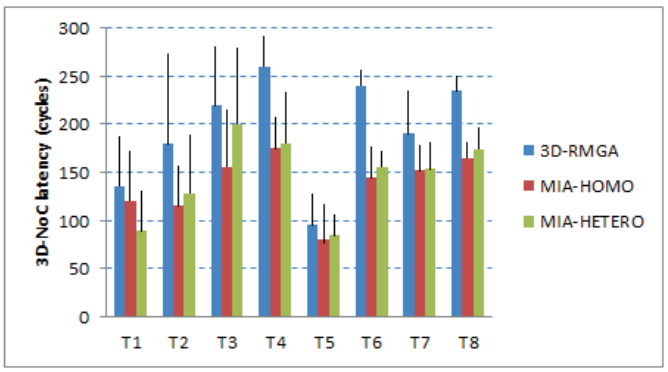

Figure 9. 3D-NoC power dynamic evaluation results.

VII. CONCLUSIONS

In this paper we propose the use of a multi-objective adaptive immune algorithm (MIA), an evolutionary approach to solve the multi-application 3D-NoC topology and mapping problem. MIA was employed to explore the 3D-NoC design space targeting the minimization of the total amount of power consumption and latency. MIA may use other objective functions. The contributions of our work include the adoption of an adaptive immune algorithm combined with the use of both, static and dynamic 3D-NoC evaluation techniques in order to solve the topology and mapping problems. For 3D-MPSoC systems, heating constraints and the multi-application characteristic must be taken into account. In this work we solve the topology and mapping problems by means of two steps: i) MIA tuning; and ii) space exploration. We analyze the sensibility of MIA over mutation rate. We show that the adaptive mutation rate can be a powerful strategy in order to enhance the performance of MIA.

As future work, we plan to evaluate the sensibility of MIA over a broader set of configuration parameters (i.e. population size). We plan to refine our analytical model in order to include a wider set of traffic characteristics (i.e. topologies, natures and types).

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