Master internship 2012 at Lab-STICC
New Networks on Chips for Neural Coding VLSI implementation

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Summary:
Neural Coding is a new and promising concept initiated by Claude Berrou and supported by Lab-STICC as a leading transversal project. The main idea is to reconsider the modelling of the human brain behavior through the prism of Information Theory instead of a classical neural-network mimetic approach. In a first stage, the proposed approach gives new solutions for the design of efficient associative memories (i.e. content based access memories) that support partial or altered (noise) input data. In a second stage, the objective will be to build machines able to create and generate new information by means of association/recombinations of stored data. The current new concept for large associative memories relies on the use of cliques and error correcting coding to store and retrieve messages from a network organised with independent clusters. It achieves performance (capacity, diversity) that overcomes the state of the art as demonstrated in V. Gripon PhD Thesis [1, 2].
The main implementation challenge for such systems is clearly the issue of communications. Network on Chips (NoC) have been proposed to solve the question of bus contention in recent Multicore System On Chip that can implement up to one hundred IPs (memory, processor, peripherals, sensors). The Lab-STICC has proposed and experienced different contributions in the domain of NoCs, such as generic CAD tools for NoCs with guarantied traffic NoCs [3], NoCs dedicated to LDPC [5] and Turbo Decoders [6], self-adaptive NoCs [7] and security-centric NoCs [4]. However the context of neural coding is radically different to existing MPSoC architectures NoCs have been designed for so far. The first aspect is the order of magnitude of the network size (e.g. 10^5 neurones, 10^2 clusters, 10^8 cliques). The flexibility needs to be drastically improved as well in order to support hierarchy and reconfigurable topologies (i.e. paths are data-dependent). The address space is large and changeable but the type of communications is also quite different since short-length but numerous and potentially periodic messages have to be efficiently supported. Finally the deletions and/or alteration of messages have to be considered. So if a network is required to interconnect such a number of nodes, current NoC solutions don't fit neural coding requirements and new ideas are necessary to cope with this emerging application domain. The aim of the master project is to investigate this unexplored research topic.

Project mains steps:
1) Study of neural coding communication requirements.
2) Analytical modelling of communications.
3) In-depth NoC study (topology, path, bit-width, packet vs circuit switching, etc.) specifically focused on the neural coding context.
4) Proposal of a cost-optimised NoC architecture compliant with neural coding requirements.
5) Cost and performance estimations.

Project duration, grant and locations:
4 to 6 months, 400€/month, Lab-STICC Brest or Lorient, France.

Expected skills:
Computer Engineering, Computer Architectures, Graph Theory, Information Theory.

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References

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[7] R. Dafali and J-Ph. Diguet, *Keys for Administration of Reconfigurable NoC: Self-Adaptive Network Interface Case Study*, in Book *Dynamic reconfigurable network-on-chip design*, IGI Global, 2009.