

Design Exploration of EMBRACE Hardware Spiking Neural Network Architecture



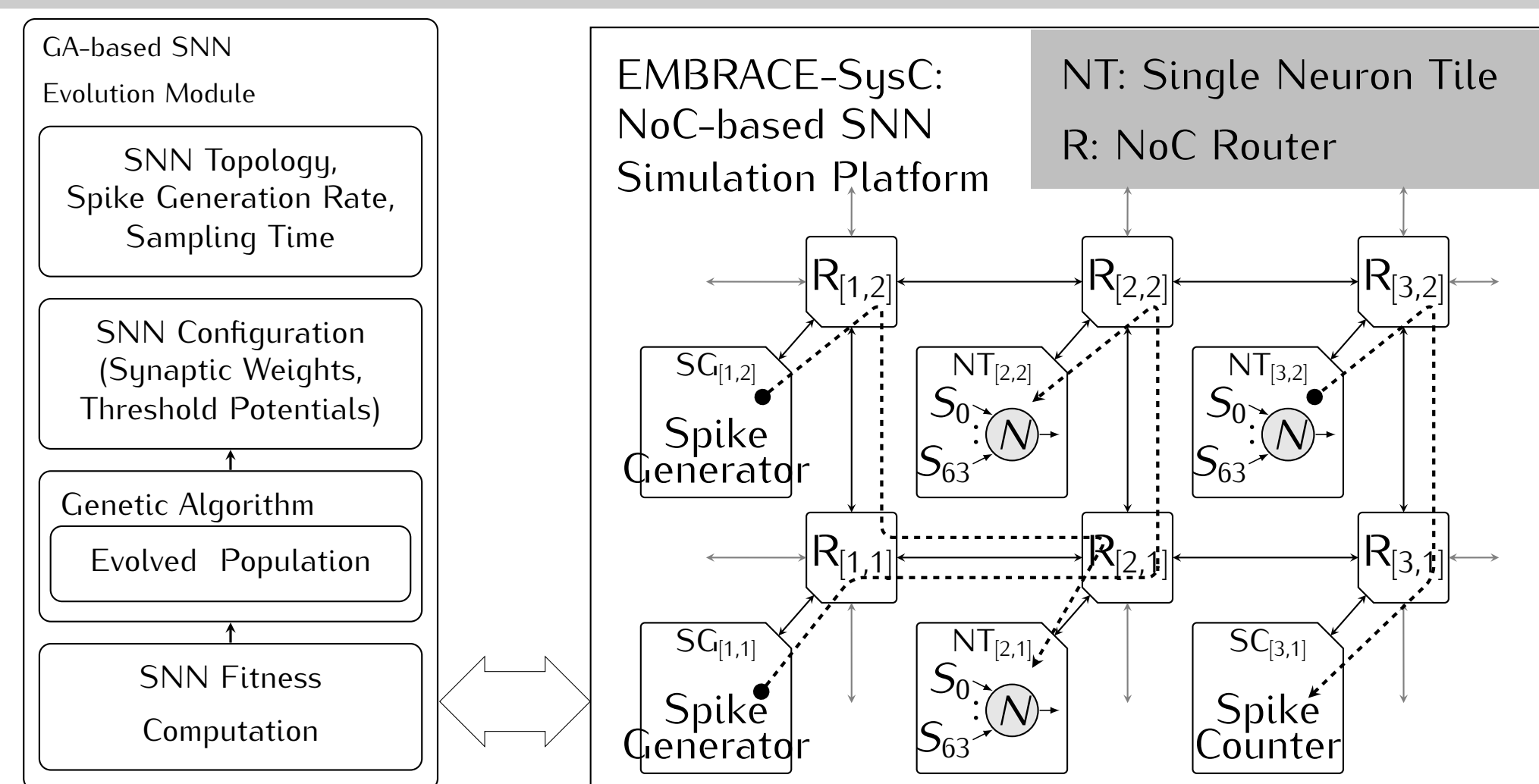
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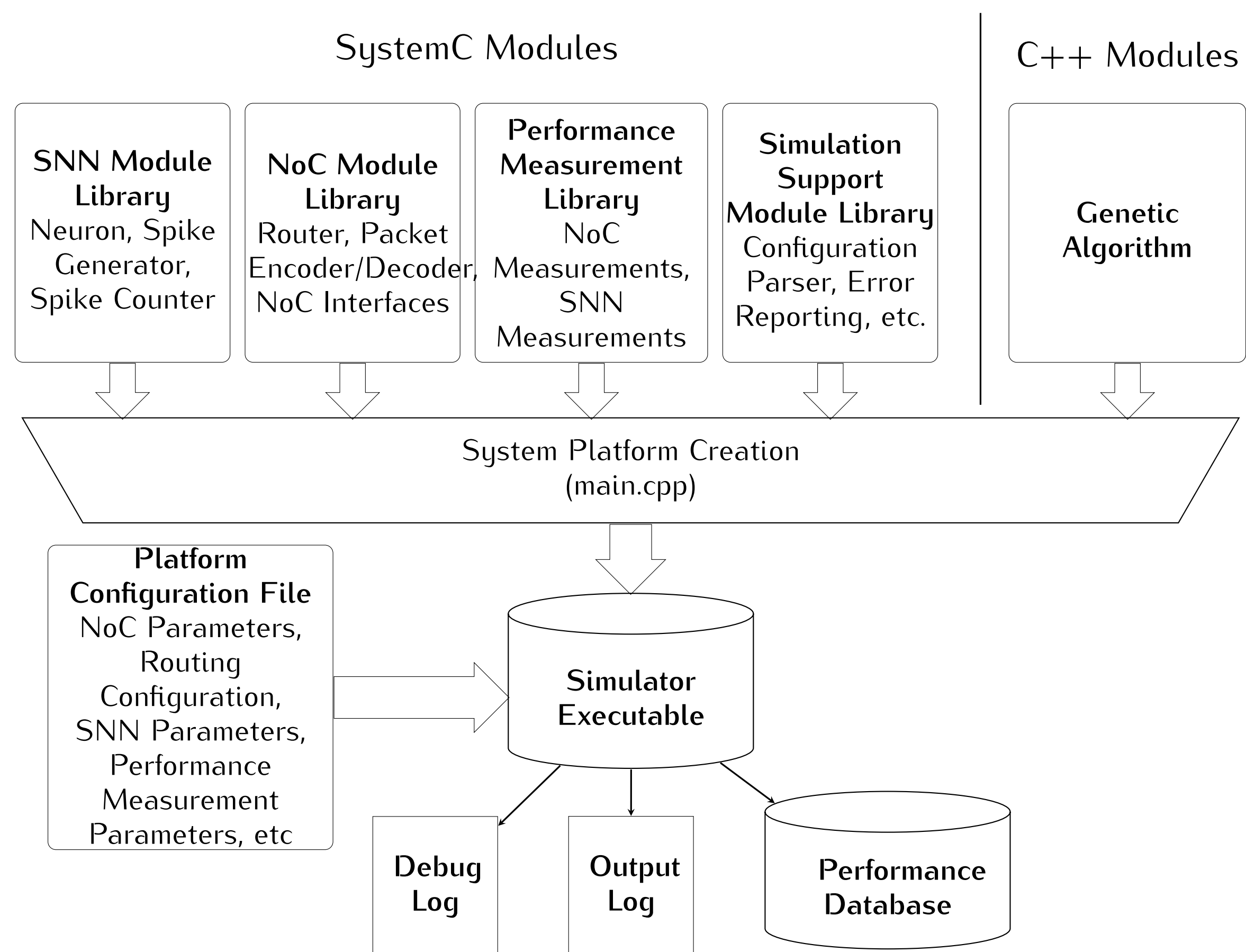
EMBRACE Hardware SNN Architecture Features

- Designed using SystemC simulation based systematic design exploration
- Compact and scalable modular neural tile design
- Low distortion hierarchical NoC architecture for reliable SNN applications
- Modular robotic navigation controller application demonstrated on EMBRACE-FPGA prototype (comprising 448 neuron and 32K synapses on Xilinx Virtex-6 XCVLX240T FPGA)

EMBRACE-SysC Design Exploration Framework



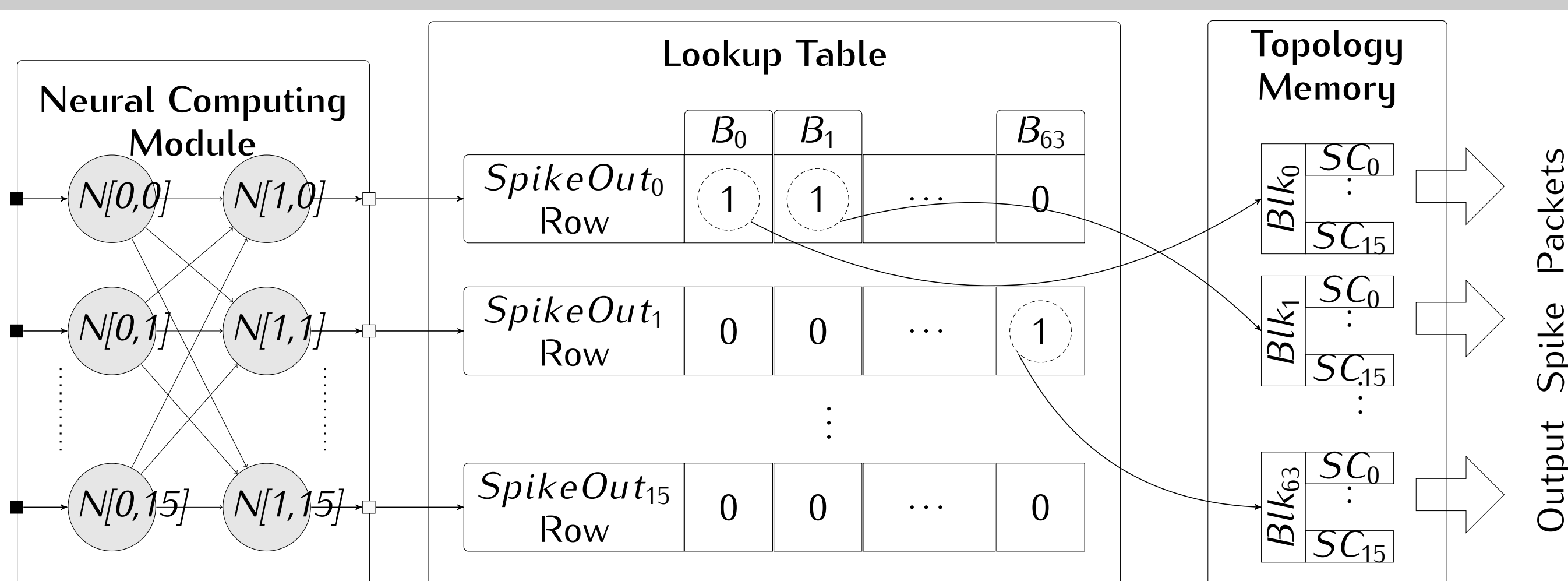
XOR Benchmark SNN Application Simulated with the EMBRACE-SysC Architecture in a 3 × 2 Mesh Configuration and GA-based SNN Evolution Module



EMBRACE-SysC Modelling and Simulation Flow

- Accurate modelling of spike data traffic and neuron circuit behaviour
- Systematic investigation of performance bottlenecks in the architecture
- Performance comparison and analysis of architectural design choices
- Evaluation of SNN application feasibility prior to hardware prototyping

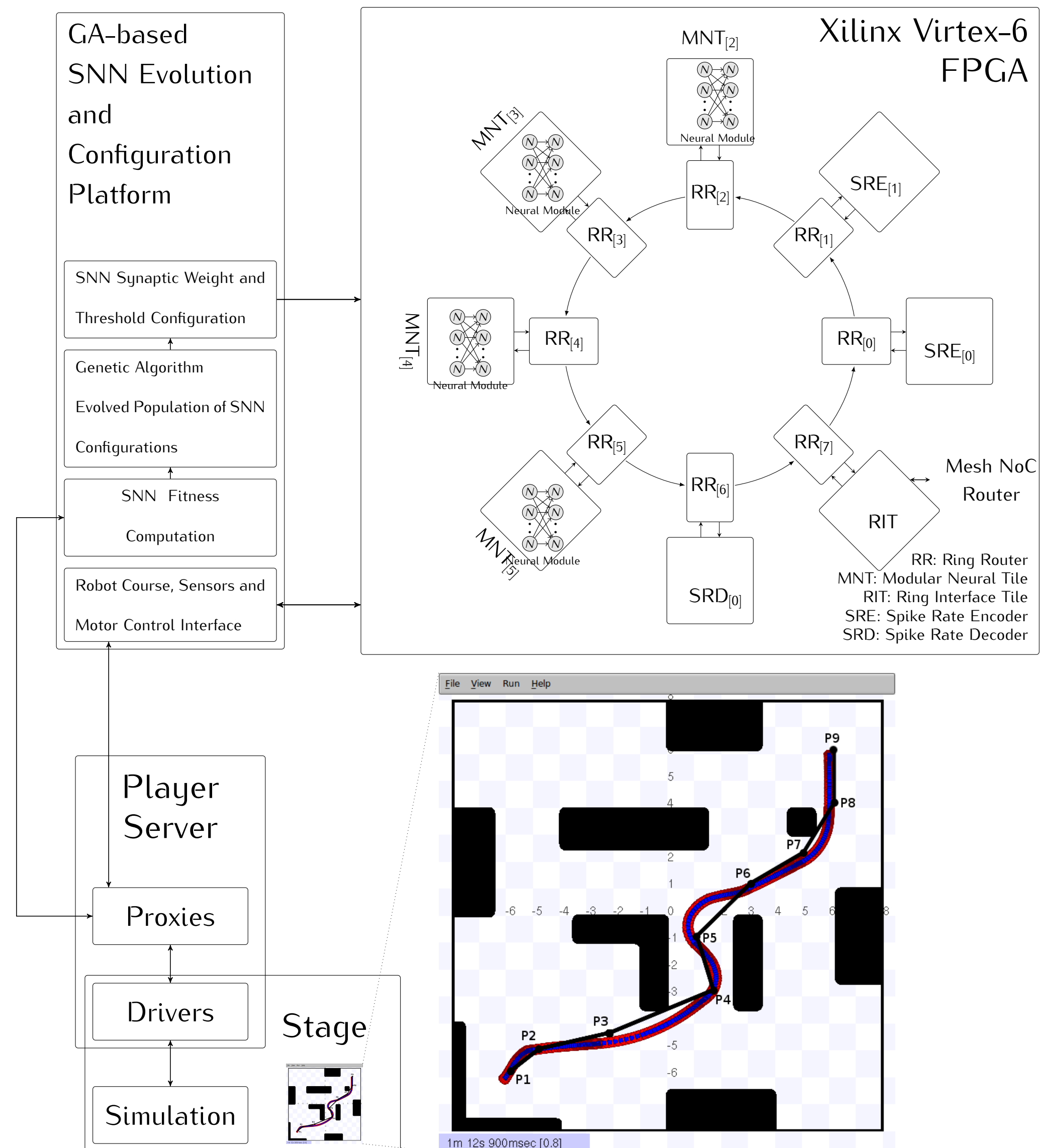
EMBRACE Modular Neural Tile Architecture



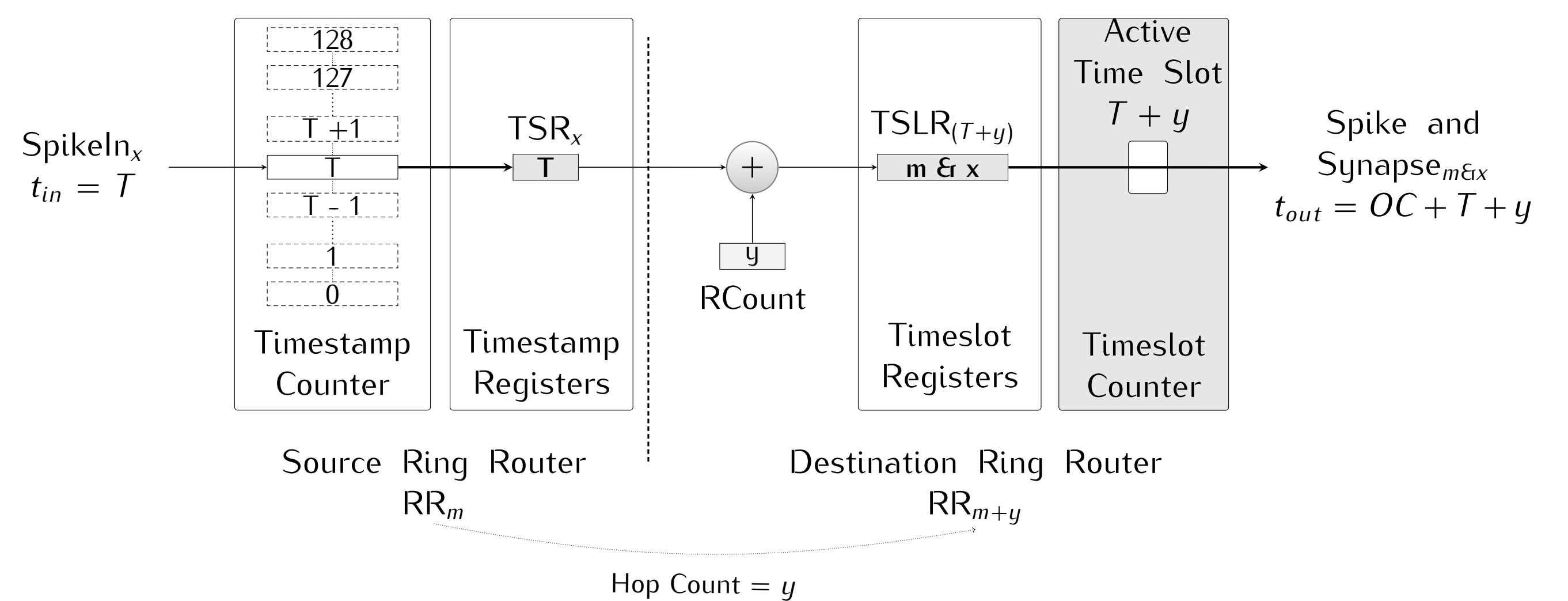
Two layered 16:16 Fully Connected SNN Structure as the Neural Computing Module and the Lookup Table-based Shared Topology Memory Organisation within the Modular Neural Tile

- Compact and scalable modular neural tile architecture for mesh topology NoC based hardware SNN
- Reduces the SNN topology memory requirement of NoC-based hardware SNNs by using a combination of fixed and configurable synaptic connections
- Average 66% reduction in silicon area requirement for practical SNN application topologies

EMBRACE Hierarchical NoC Architecture



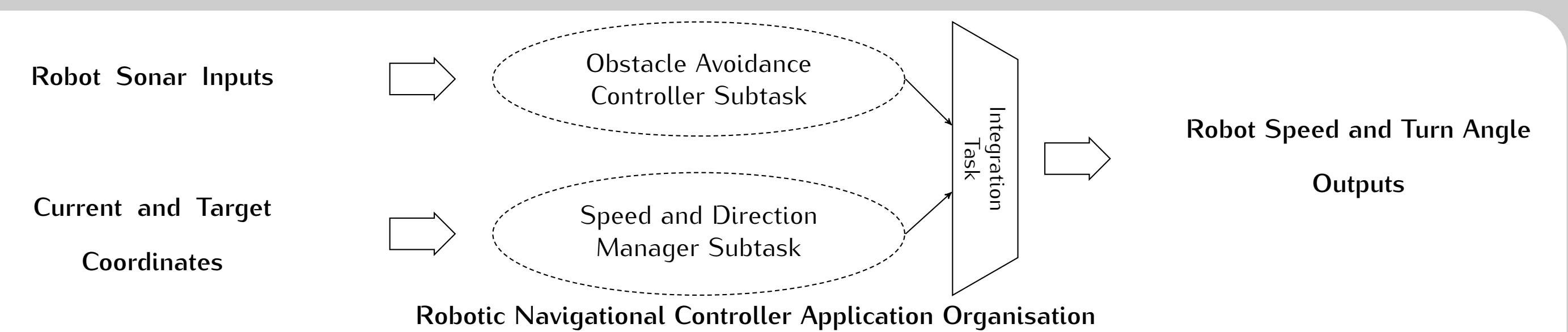
Robotic Controller Evolution Setup Comprising Ring Topology EMBRACE-FPGA Prototype, GA-based SNN Evolution Platform and Player-Stage Robotic Simulation Environment



Fixed Latency Spike Packet Flow Control

- Fixed spike transfer latency ring interconnect within mesh topology NoC architecture
- Novel timestamped broadcast flow control offering high density localised spike transfer
- Eliminates SNN information distortion due to NoC spike latency jitter
- Insures reliable SNN application behaviour for various NoC traffic conditions

Modular Robotic Navigational Controller Application



Robotic Navigational Controller Application Organisation

- Complex multifunctional robotic navigational controller application decomposed into:
 1. Obstacle avoidance controller subtask controls the robot movement for avoiding obstacles
 2. Speed and direction manager subtask steers the robot towards target location
- Application partitioning based on sensory inputs and functionality
- Modular application prototyping technique offers:
 - Simplified SNN training
 - Faster application evolution
 - Accurate application behaviour
 - Stepwise knowledge integration

References

1. Sandeep Pande, et al., Embrace-sysc for analysis of NoC-based spiking neural network architectures, International Symposium on System on Chip (SoC), Sept. 2010, Tampere, Finland.
2. Sandeep Pande, et al., Addressing the hardware resource requirements of Network on Chip based neural architectures, in NCTA, International Conference on Neural Computation Theory and Applications, Oct. 2011.
3. Sandeep Pande, et al., Modular neural tile architecture for compact embedded hardware spiking neural network, Special Issue of Neural Processing Letters journal, 2011.
4. Sandeep Pande, et al., Fixed latency on-chip interconnect for hardware spiking neural network architectures, Journal of Parallel Computing, Special Issue on Novel On-Chip Parallel Architectures and Software Support, 2013 (Under review).
5. Sandeep Pande, et al., Application prototyping for EMBRACE hardware modular spiking neural network architecture, Neural Computing and Applications Journal, 2013 (Under review).