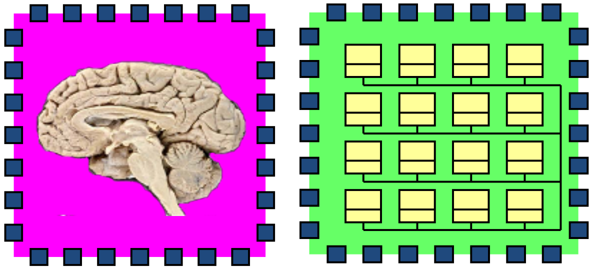

SpiNNaker

- a Biologically-Inspired Massively-Parallel Architecture

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DATE 22 Mar 2013

Bio-inspiration

- How can massively parallel computing resources accelerate our understanding of brain function?
- How can our growing understanding of brain function point the way to more efficient parallel, fault-tolerant computation?

SpiNNaker
Biologically Inspired Massively Parallel Architectures

Building brains

- Brains demonstrate
  - massive parallelism (10^{11} neurons)
  - massive connectivity (10^{15} synapses)
  - excellent power-efficiency
  - much better than today's microchips
  - low-performance components (~ 100 Hz)
  - low-speed communication (~ metres/sec)
  - adaptivity – tolerant of component failure
  - autonomous learning

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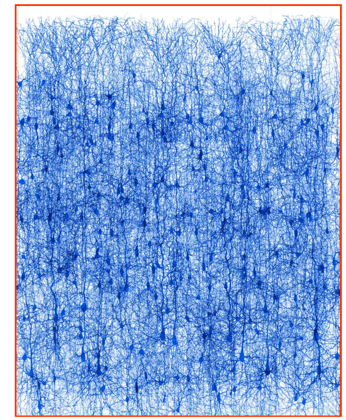
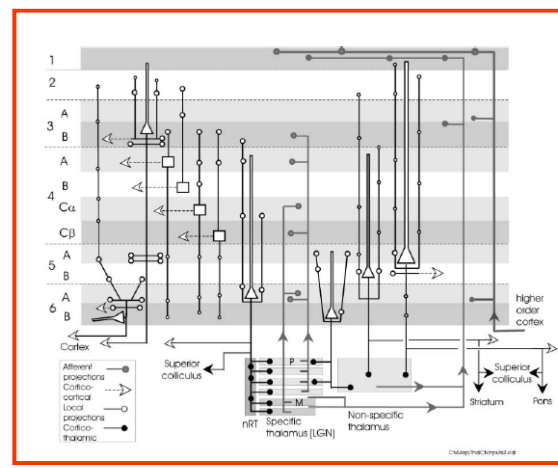
SpiNNaker
Biologically Inspired Massively Parallel Architectures

Building brains

- Neurons
  - multiple inputs, single output (c.f. logic gate)
  - useful across multiple scales (10^2 to 10^{11})
- Brain structure
  - regularity
  - e.g. 6-layer cortical ‘microarchitecture’





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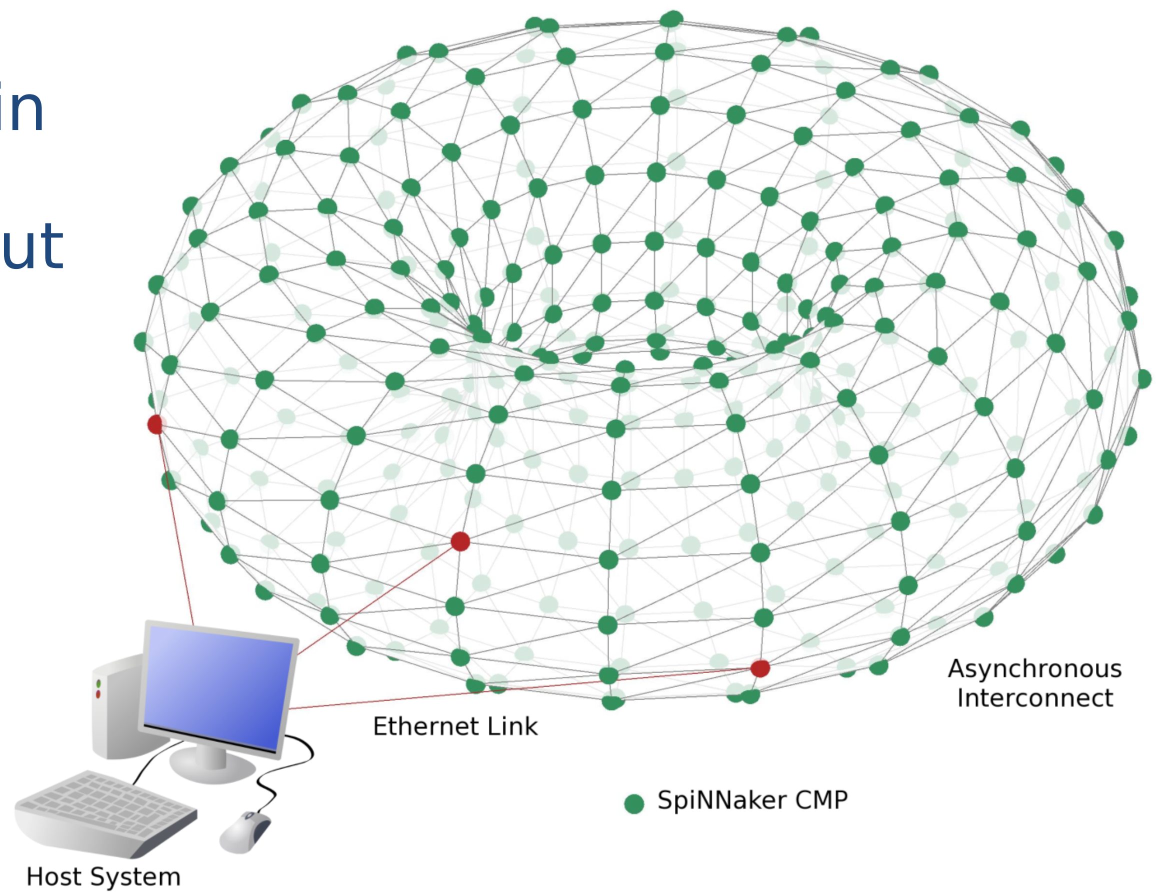
Design principles

- *Virtualised topology*
  - physical and logical connectivity are decoupled
- *Bounded asynchrony*
  - time models itself
- *Energy frugality*
  - processors are free
  - the real cost of computation is energy

Building machines

- A million mobile phone processors in one computer
- Able to model about 1% of the human brain…
- …or 10 mice!



SpiNNaker
Biologically Inspired Massively Parallel Architectures

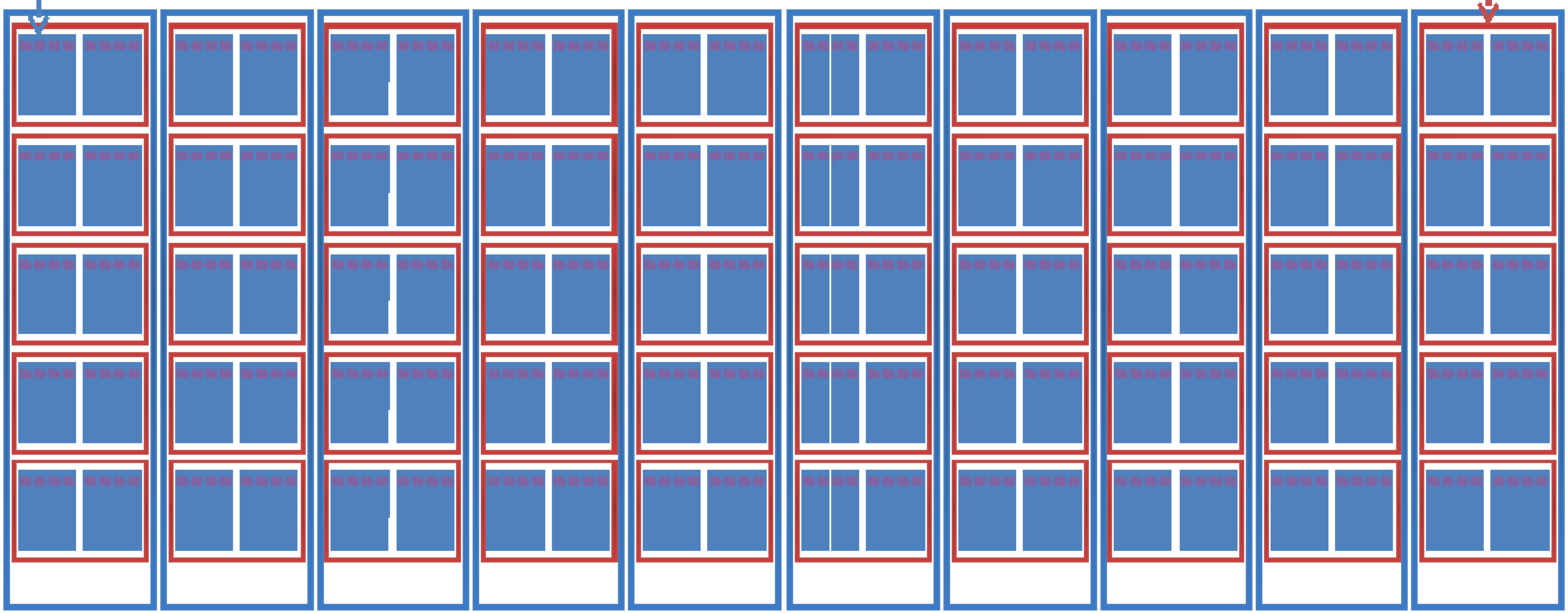
Building machines

103 machine: 864 cores, 1 PCB, 75W

104 machine:10,368 cores, 1 rack, 900W
(NB 12 PCBs for operation without aircon)

105 m/c: 103,680 cores, 1 cabinet, 9kW

106 m/c: 1M cores, 10 cabs, 90kW



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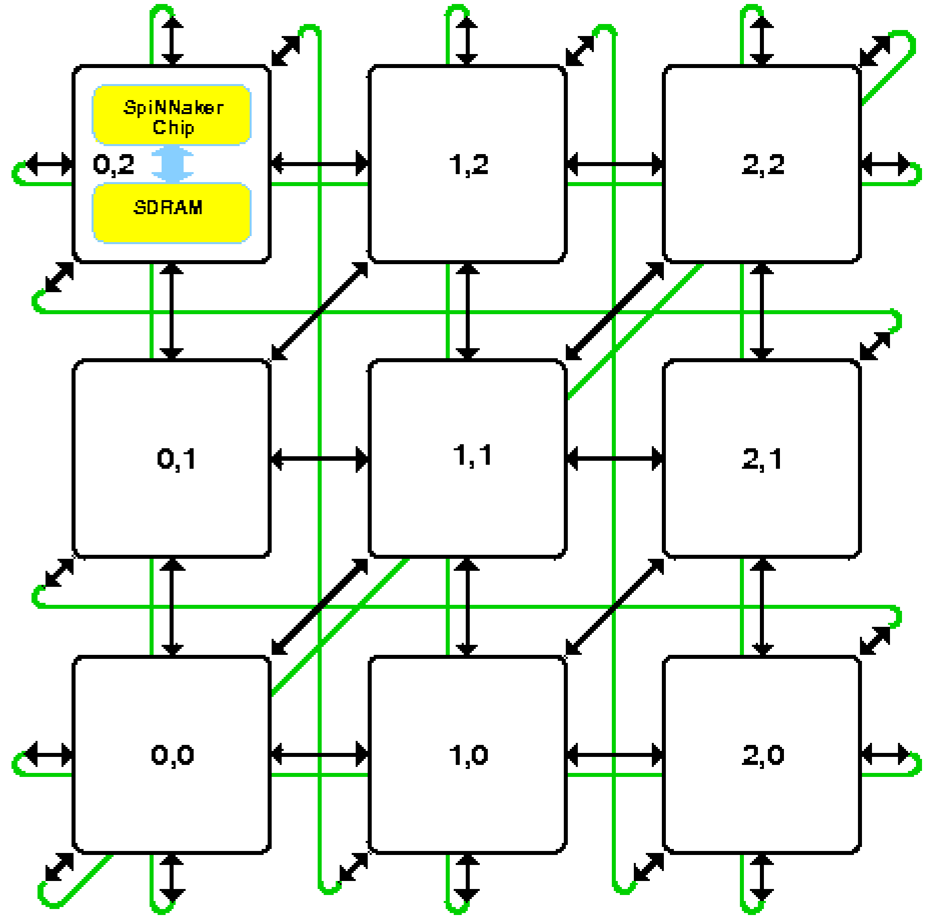
SpiNNaker system

SpiNNaker
Biologically
Inspired
Massively
Parallel
Architectures

- A packet-switched, toroidal hexagonal grid of chips
- A routable network with virtual topology
- Each chip: 16 Application Cores, 1 Monitor, 1 Spare
- Each package: SpiNNaker die + SDRAM



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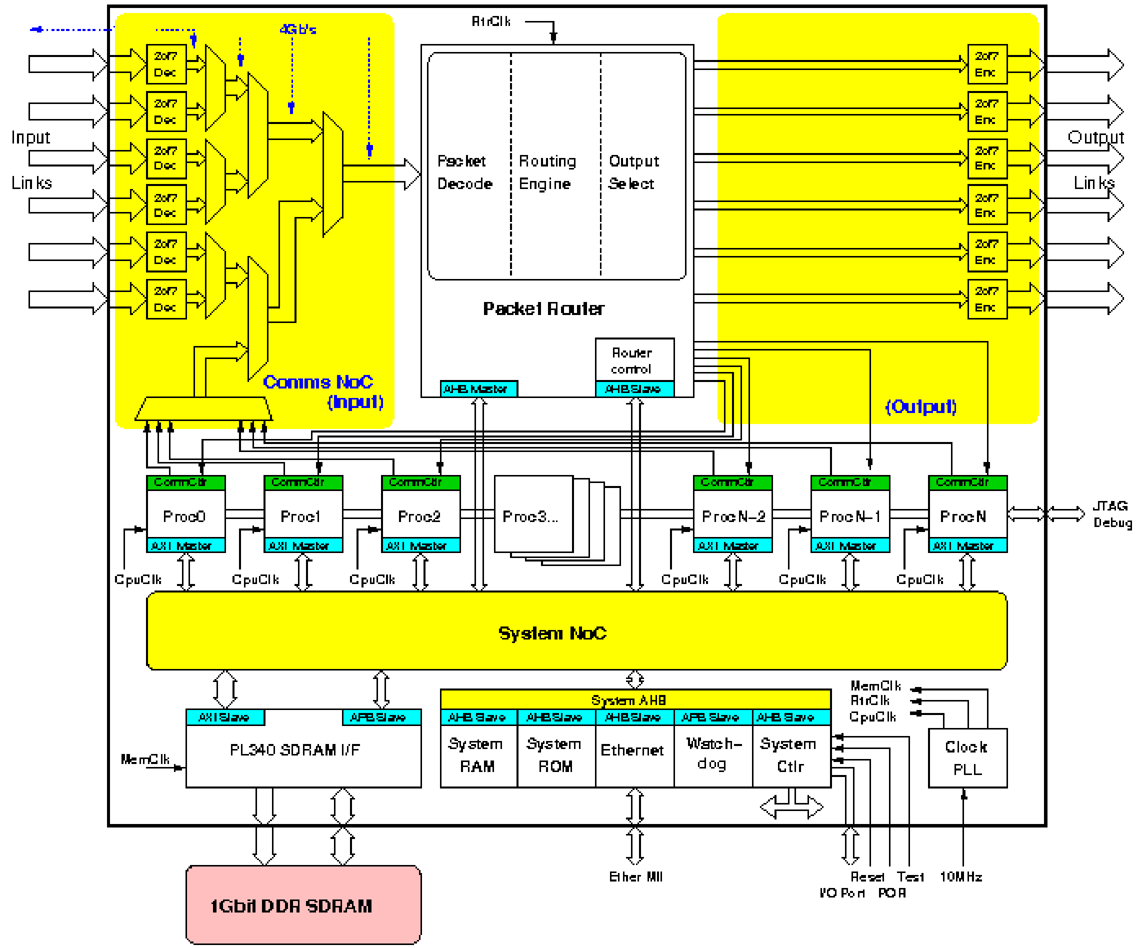
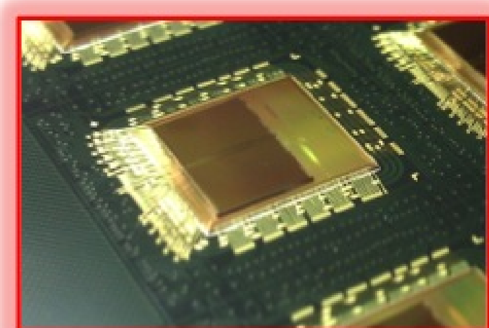
SpiNNaker node

- Native parallelism
- Event-driven Processing
- Distributed Incoherent Memory
- Incremental Reconfiguration



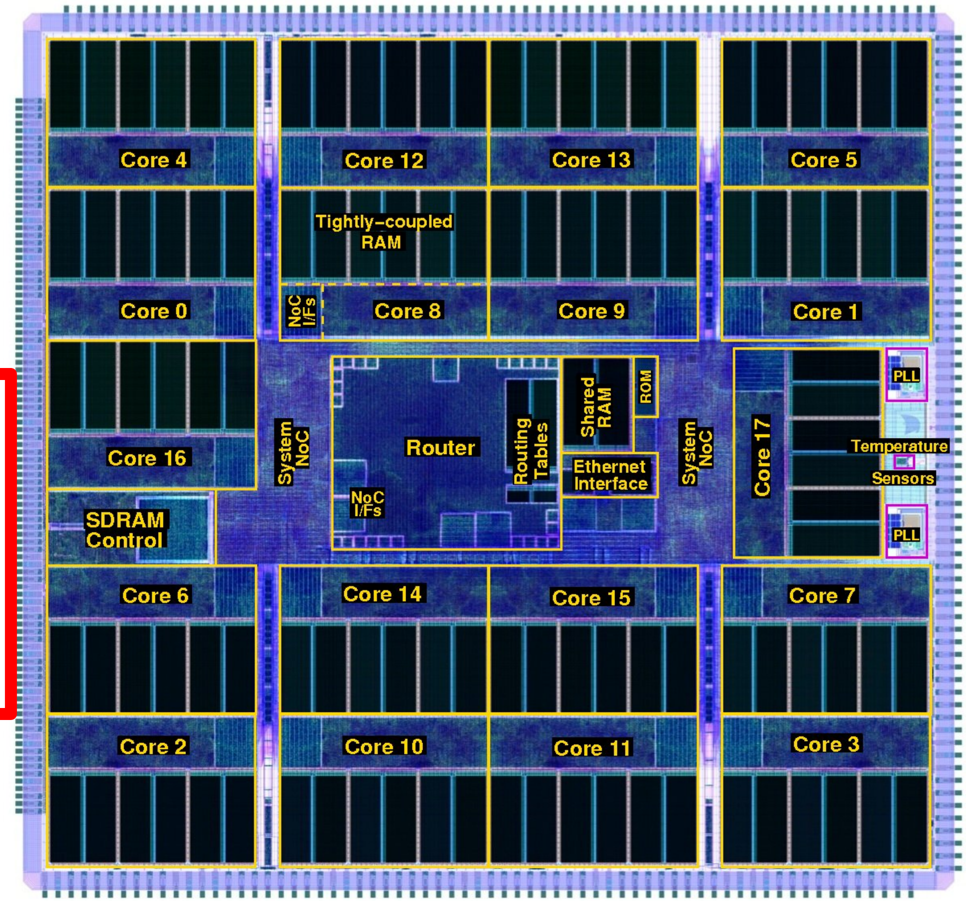
SpiNNaker
Biologically Inspired Massively Parallel Architectures

SpiNNaker chip

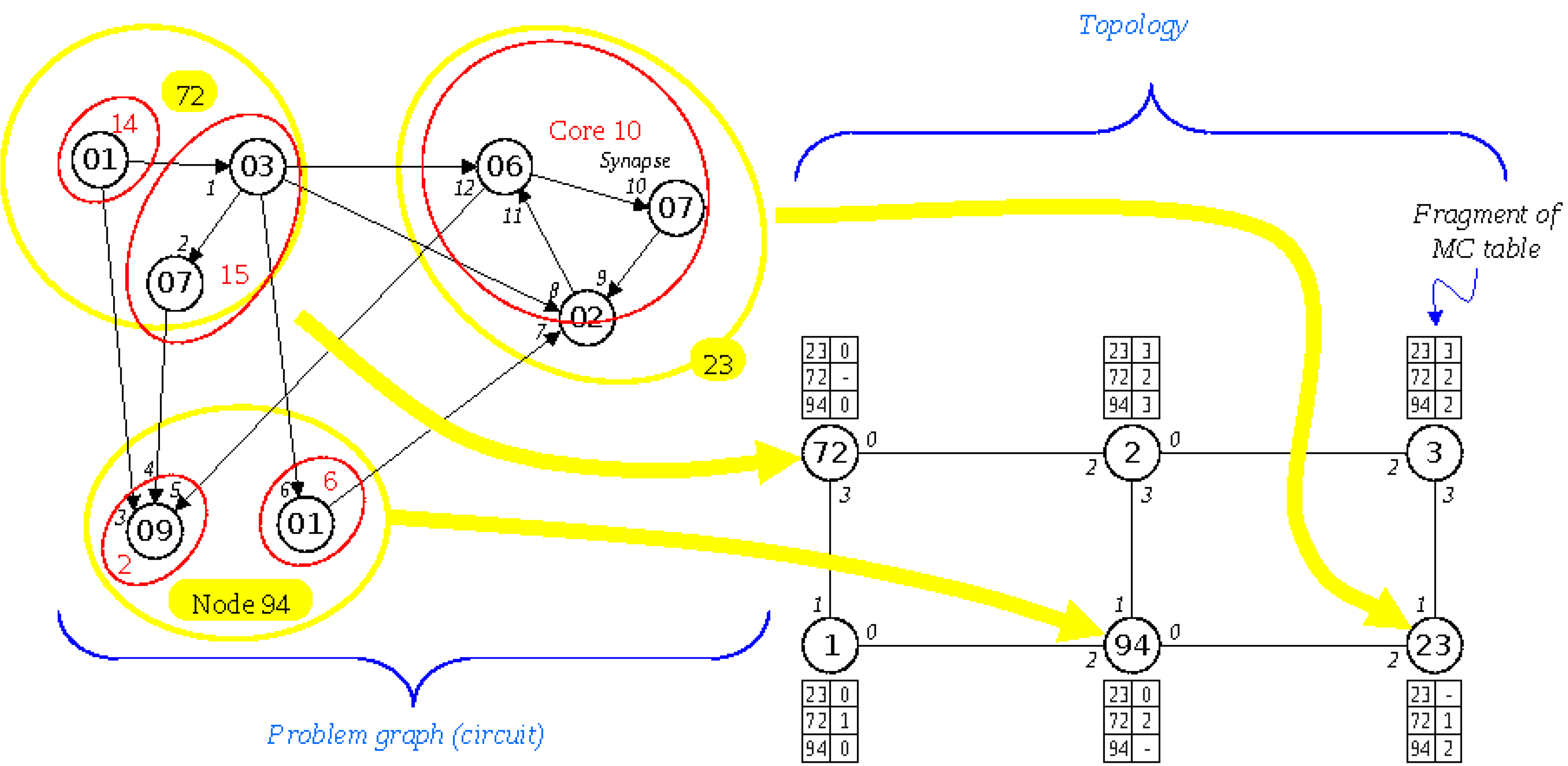


Multi-chip packaging by UNISEM Europe

Mobile DDR SDRAM interface

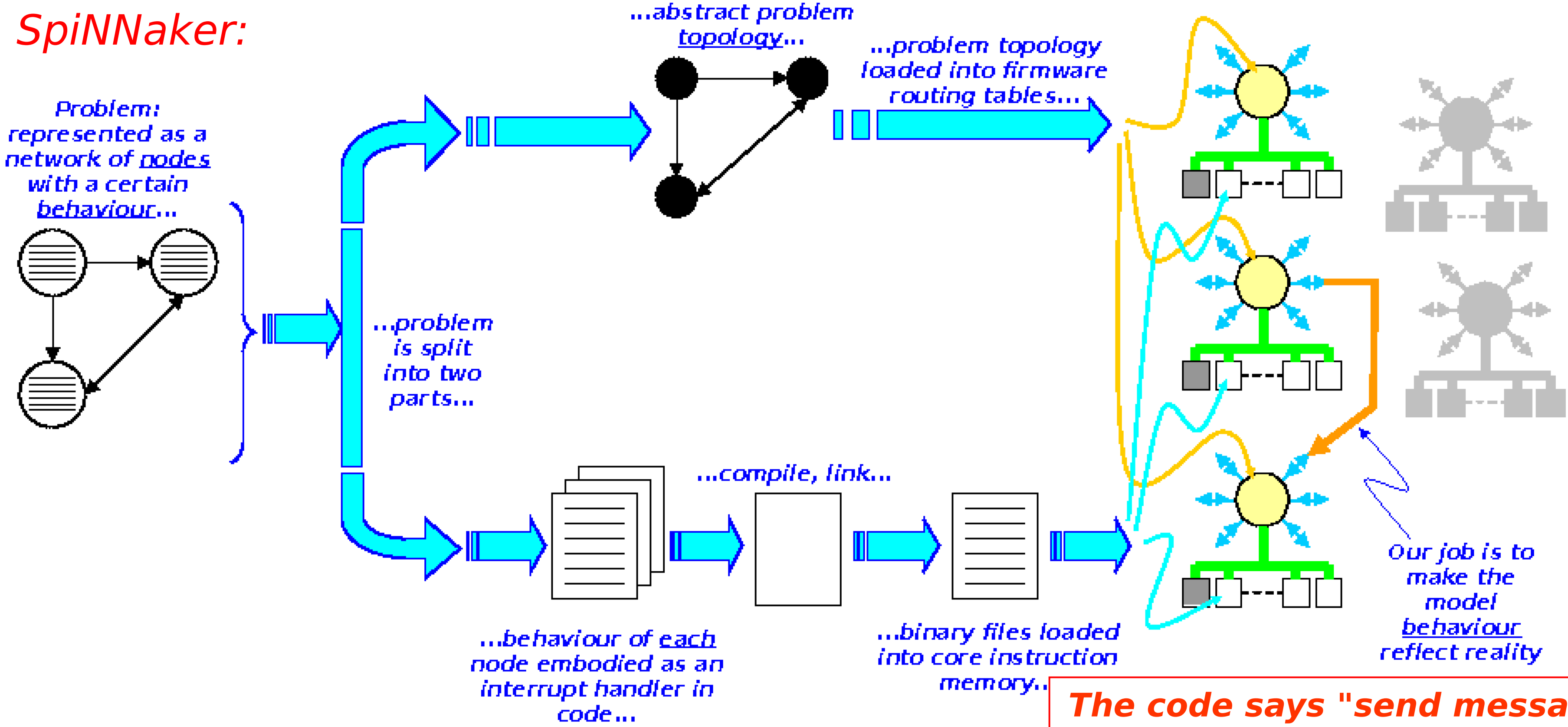


Topology mapping



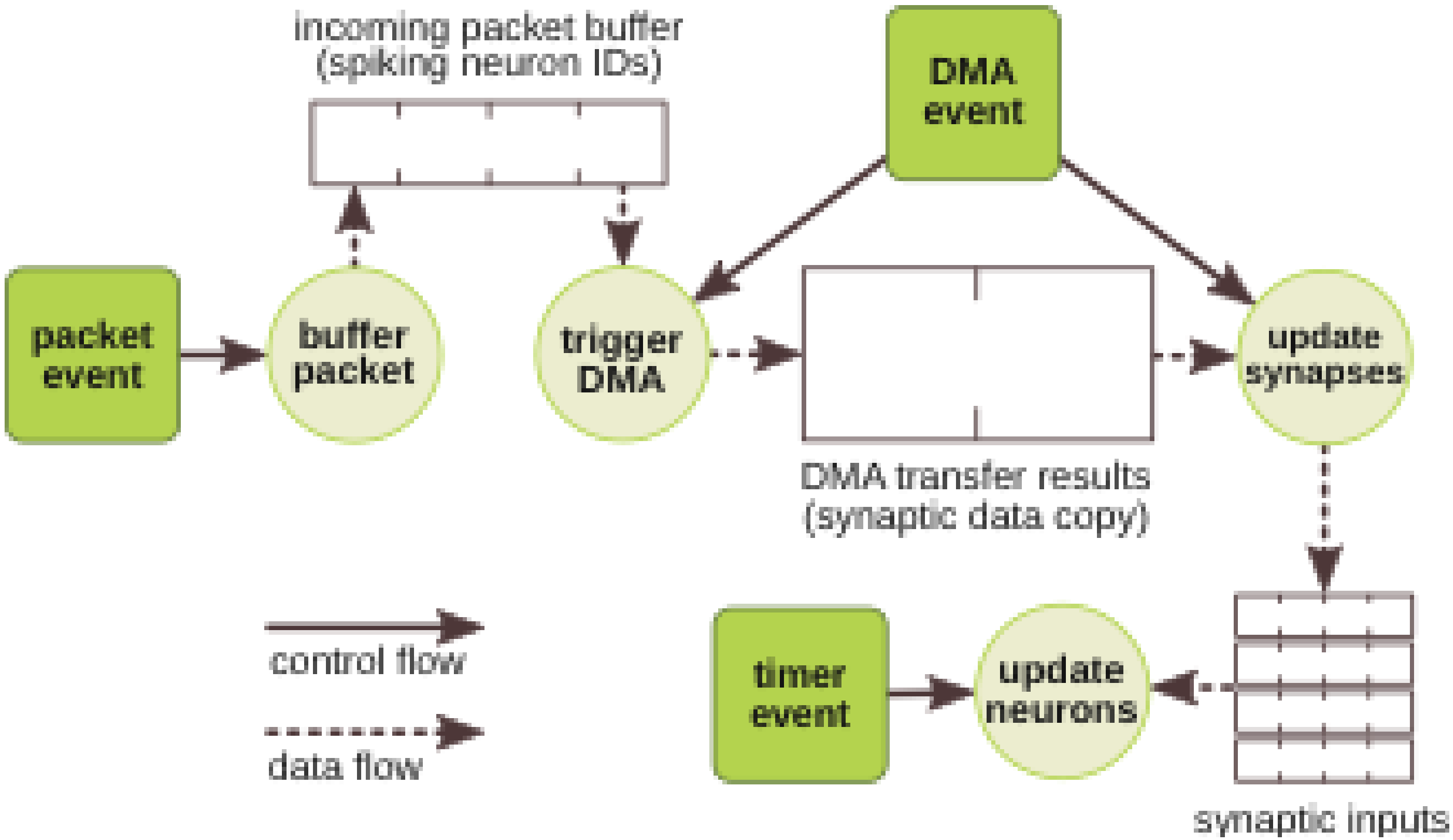
Problem mapping

SpiNNaker:



The code says "send message" but has no control where the output message goes

Event-driven software model



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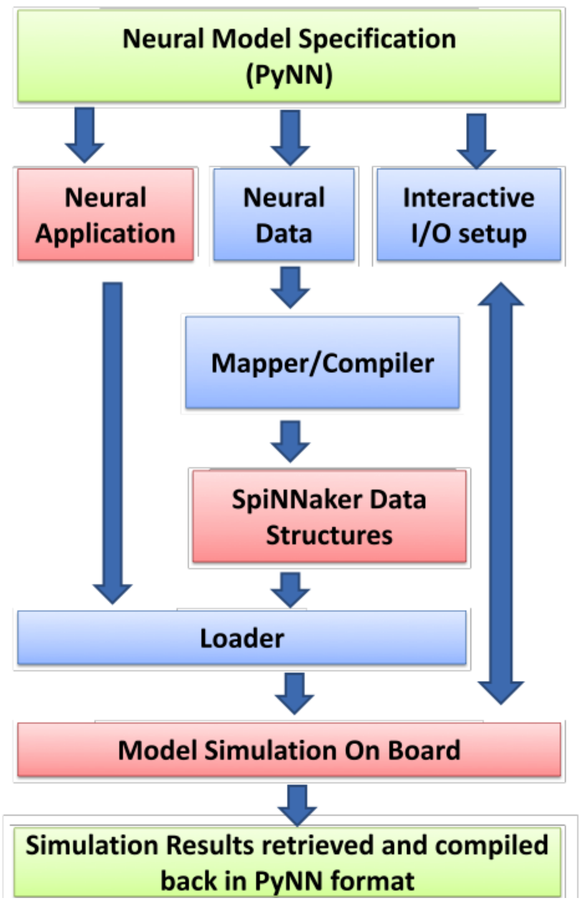
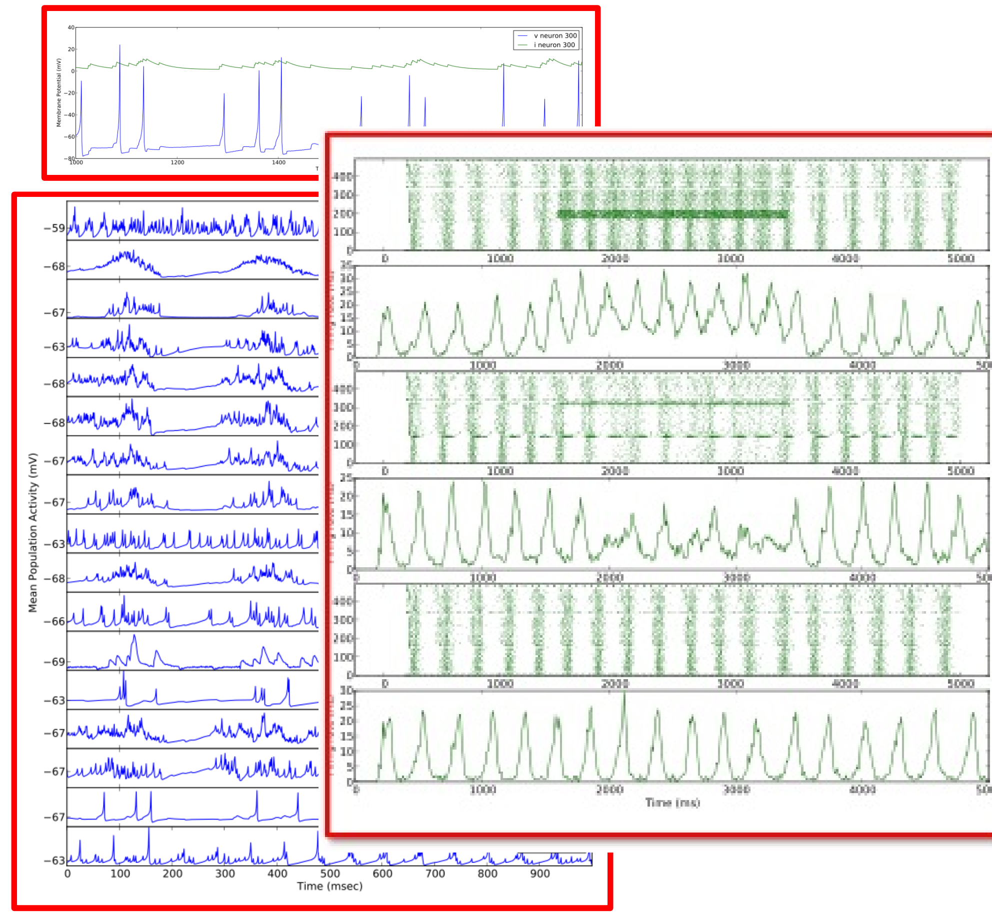
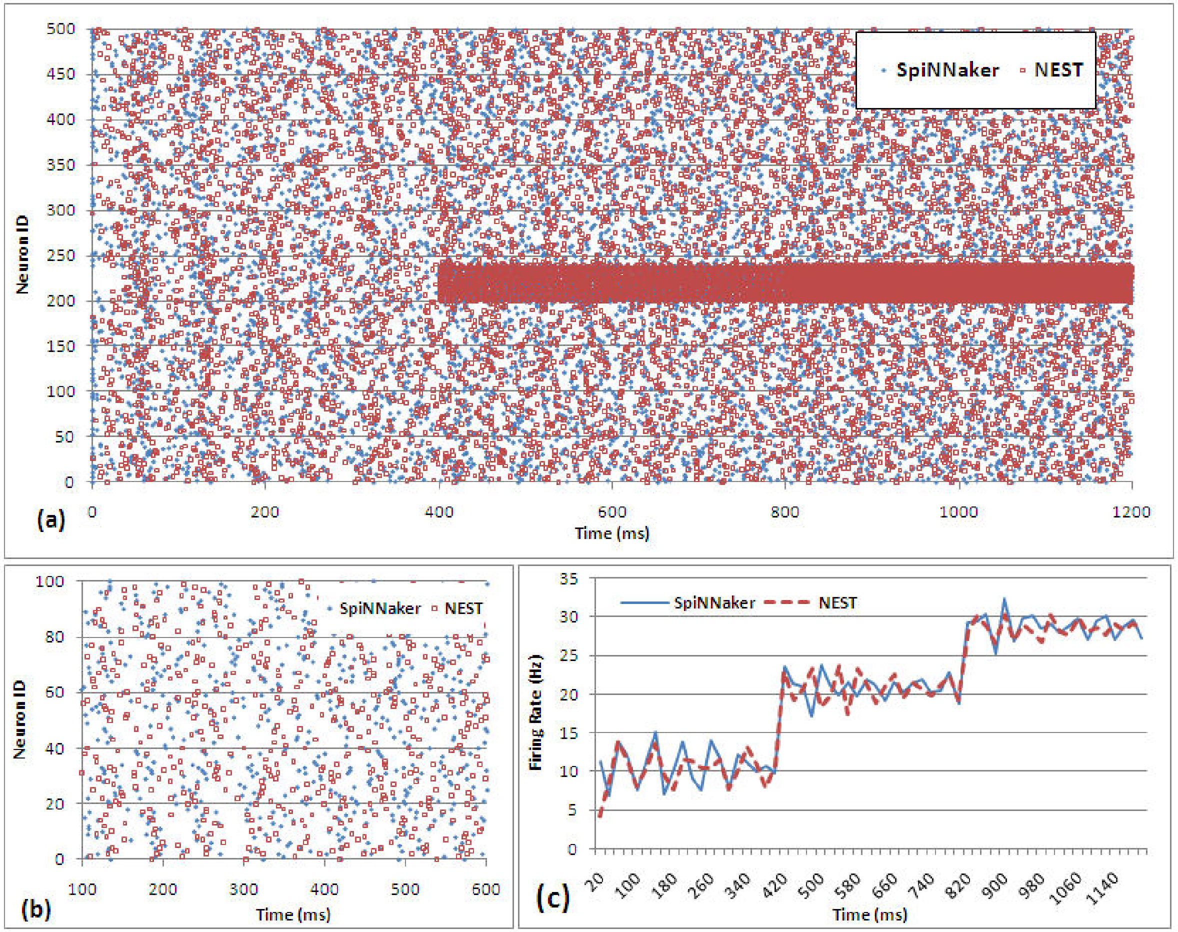
PyNN design flow





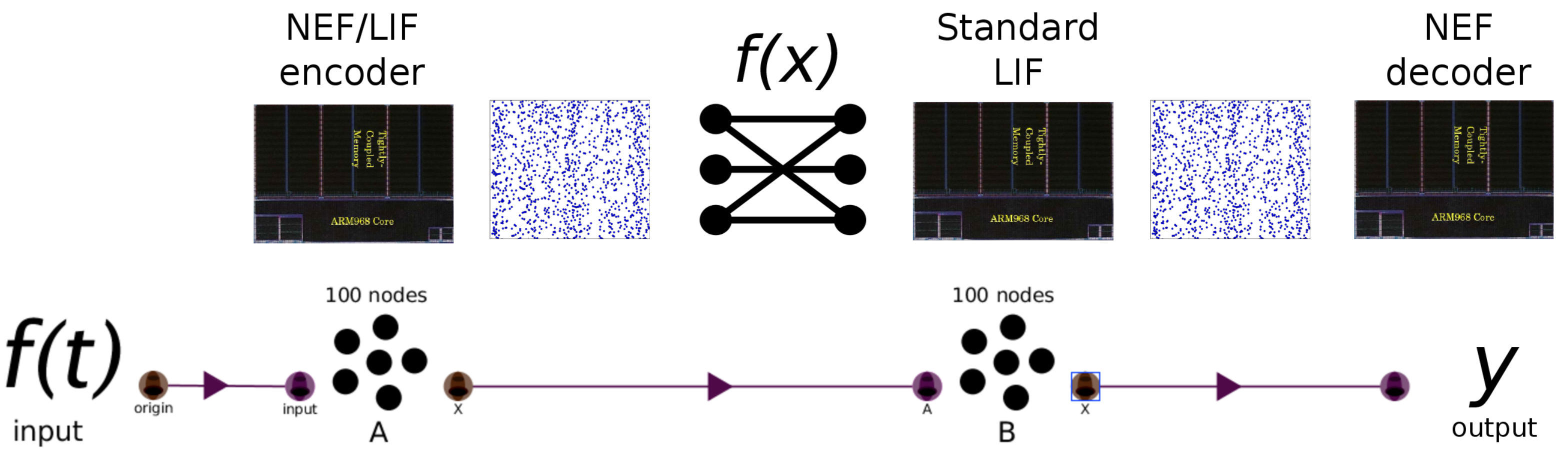
PyNN integration

- Vogels-Abbott benchmark
  - 500 LIF neurons

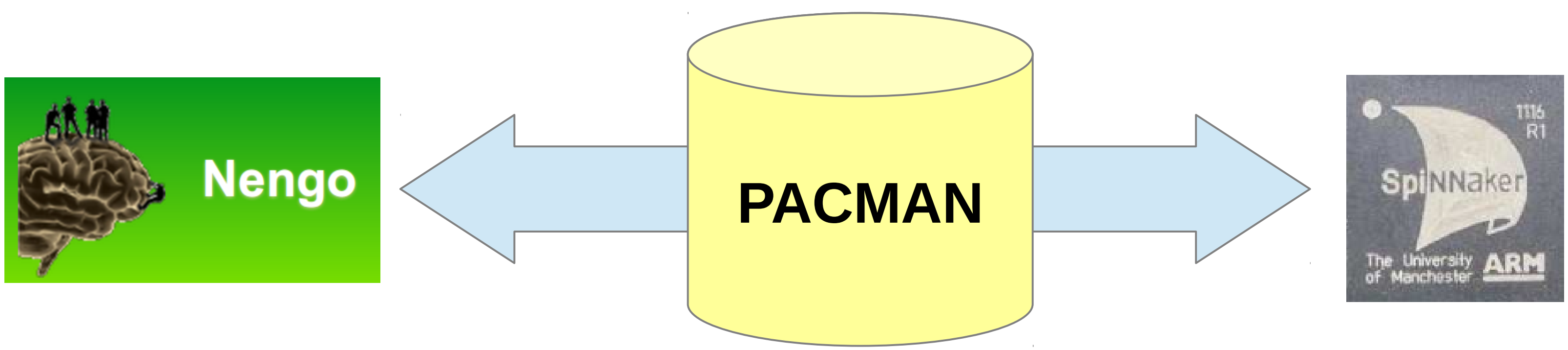


DATE 22 Mar 2013

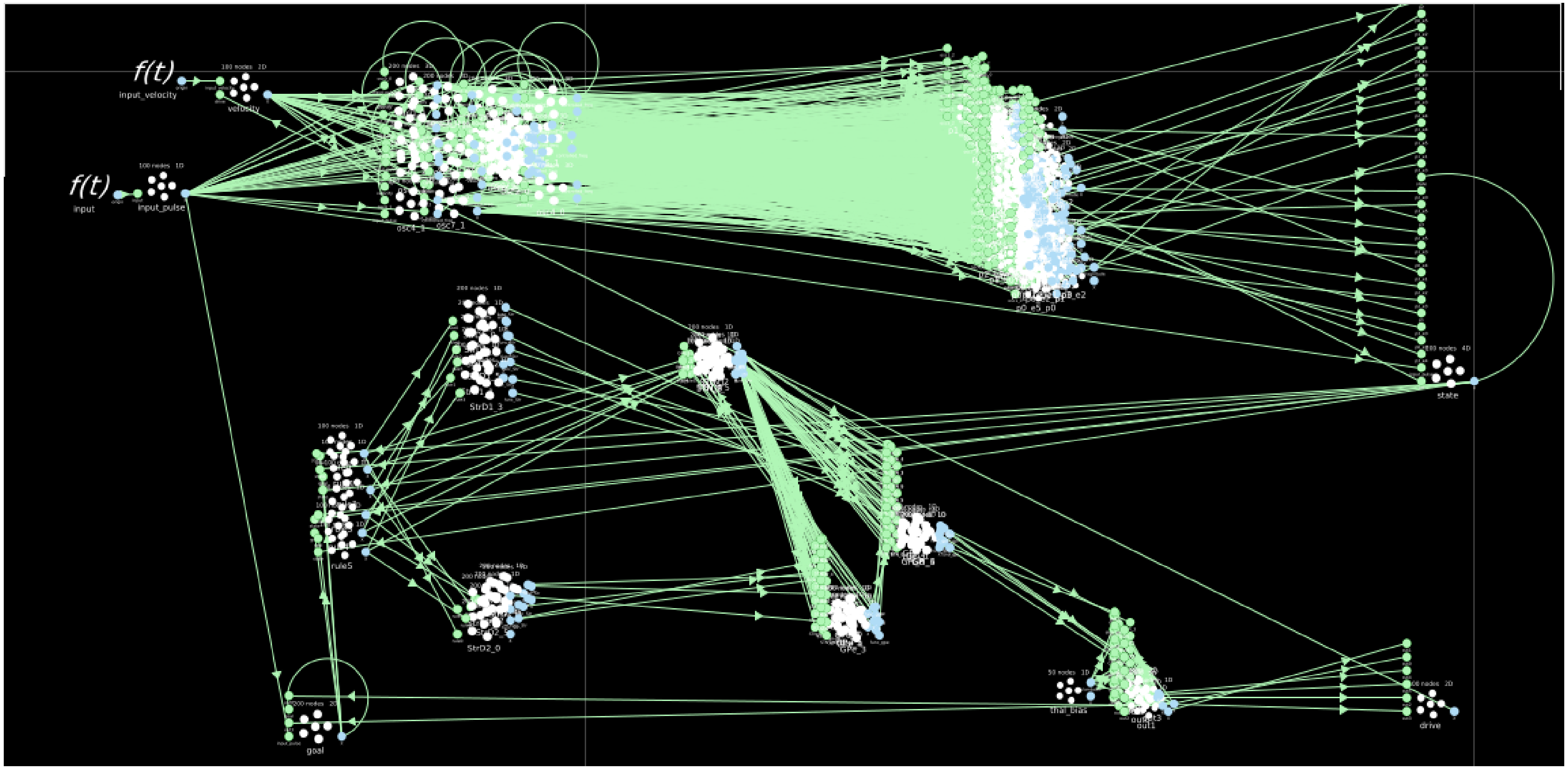
Nengo integration



• Models are written in Nengo and automatically translated into SpiNNaker data structure by PACMAN. Real time interaction using Nengo



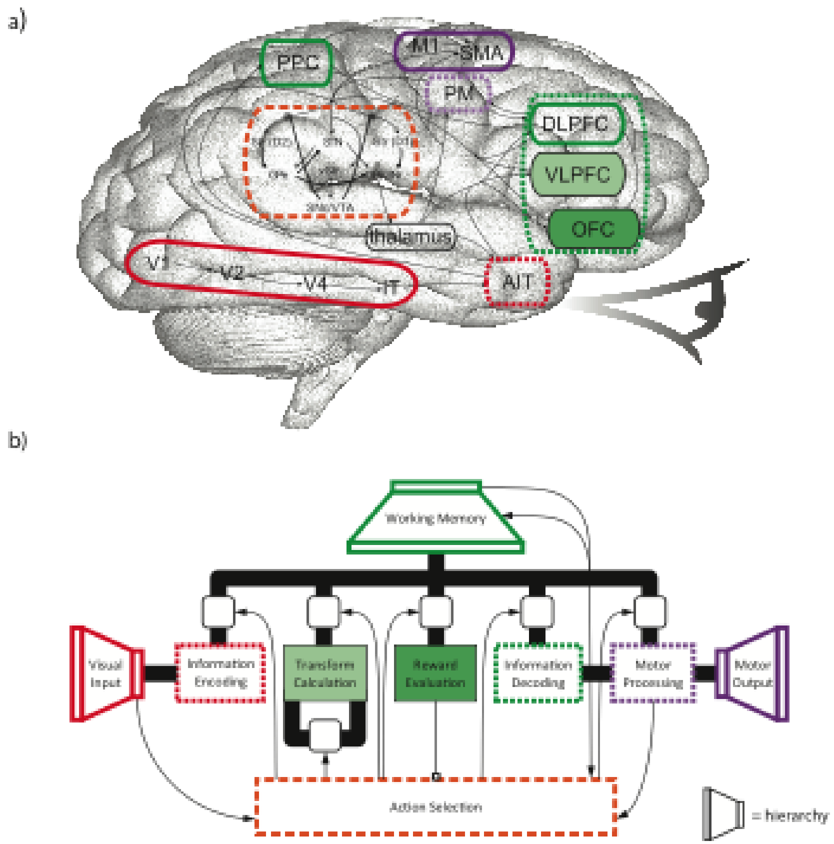
NENGO Spiking ratSLAM



- 13910 neurons in 230 populations - 670 SpiNNaker cores
- 4806500 synapses in 1601 projections - 40-100 Hz firing rate

Spaun

- SpiNNaker:
  - 5M conn/s/ARM
- Spaun:
  - 2.5M neurons
  - ~100Hz firing rates
  - ~500 inputs/neuron
  - 125G conn/s
- Real-time Spaun:
  - 25,000 ARMs
  - 30x 48-node PCB
  - by end 2013?



Chris Eliasmith et al, Science vol. 338, 30 Nov 2012

Conclusions

- Brains represent a significant computational challenge
  - now coming within range?
- *SpiNNaker* is driven by the brain modelling objective
  - virtualised topology, bounded asynchrony, energy frugality
- The major architectural innovation is the multicast communications infrastructure
- We have working hardware
  - 48-node 864-ARM PCBs now
  - first multi-PCB systems now working