Hierarchical event-based reconfigurable systems for cognitive neuromorphic engineering

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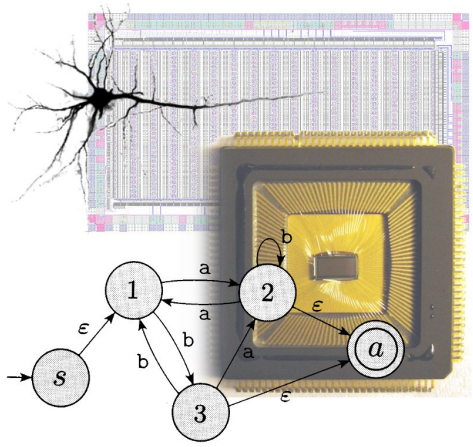
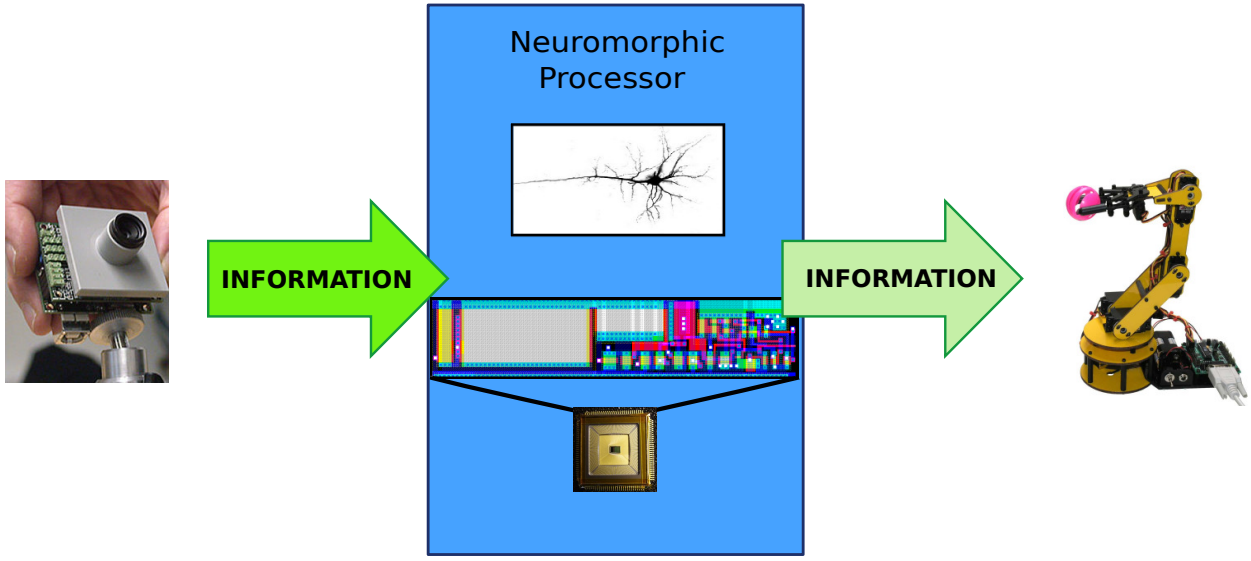


Neuromorphic Information processing systems



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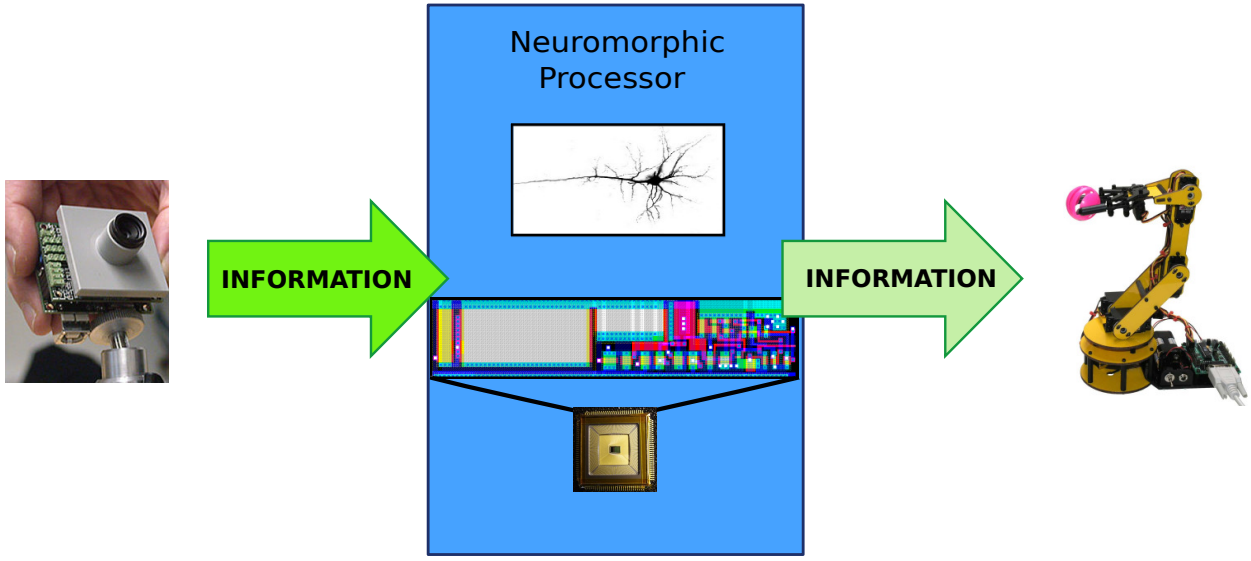


Computation

A “cognitive” task

e.g. Recognize gesture/speech, Play poker, 2AFC

Algorithm

?

Implementation

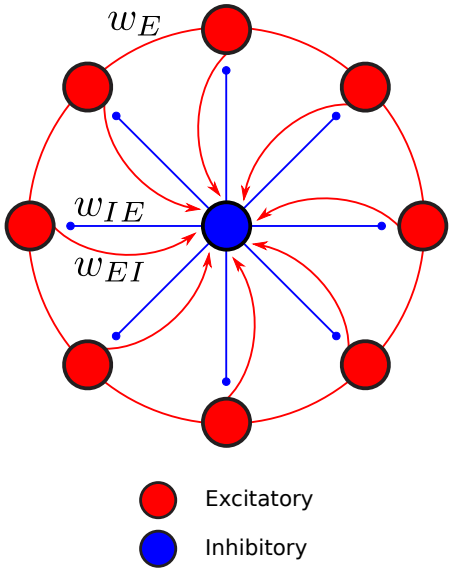
Noisy and heterogenous VLSI spiking neurons

A *middle-out* approach (?, ?)

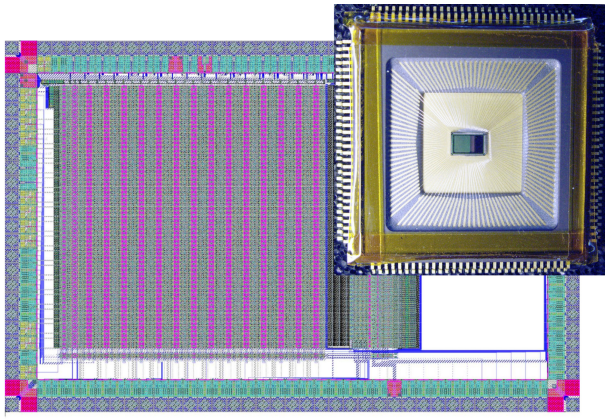
Cognitive task

The Soft Winner-Take-All (SWTA) Network

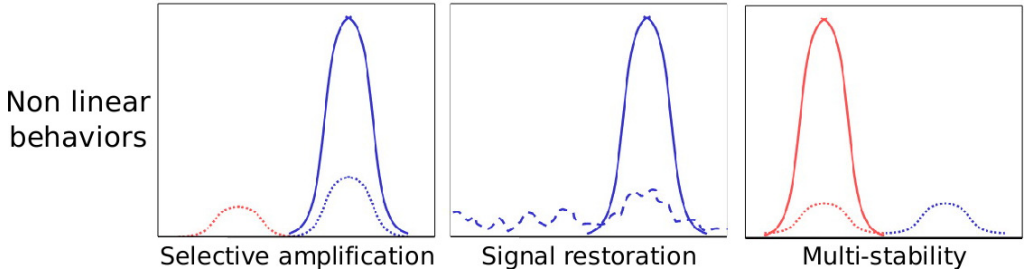
sWTA network



Neuromorphic implementations of sWTA



(?, ?)



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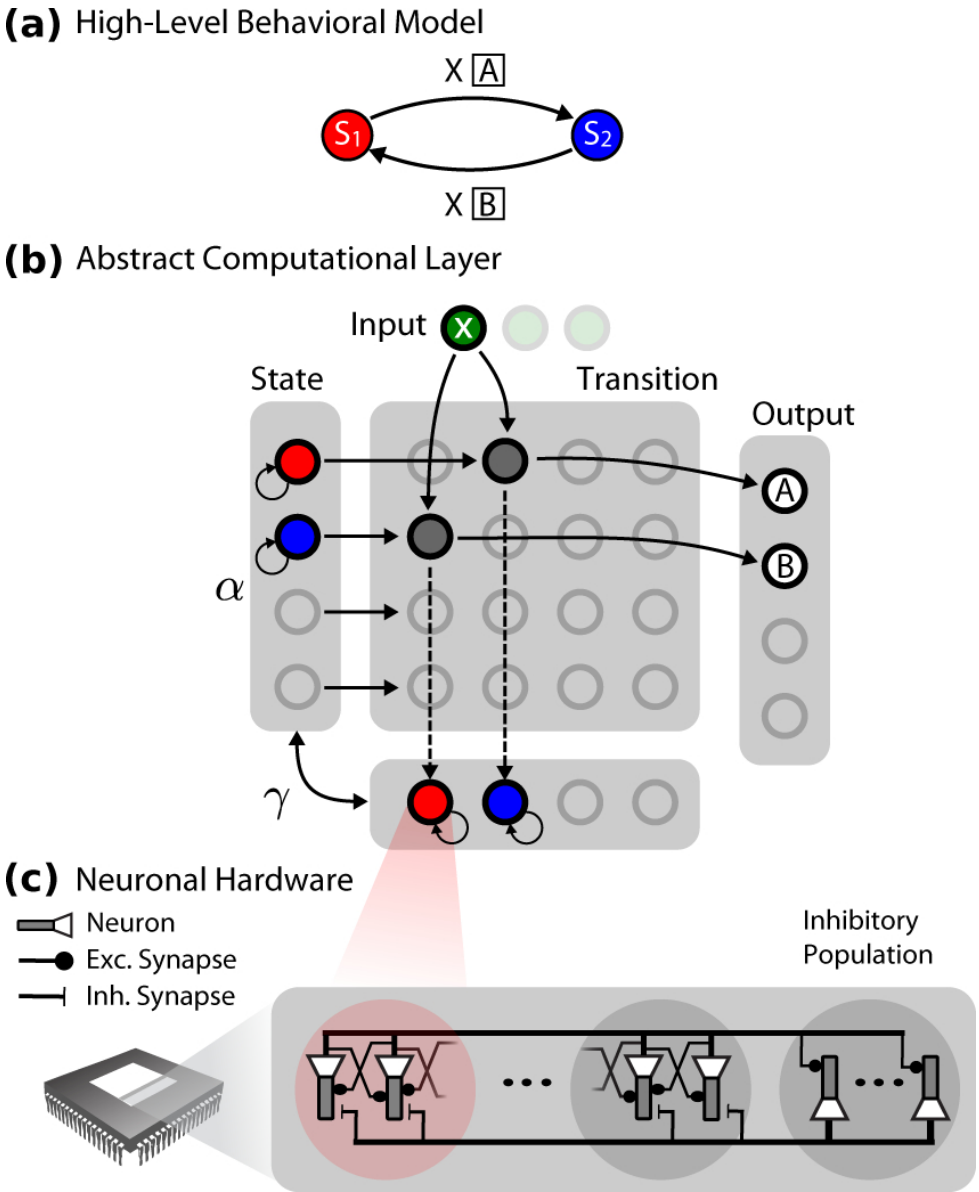
Soft WTA as primitives for general-purpose computation

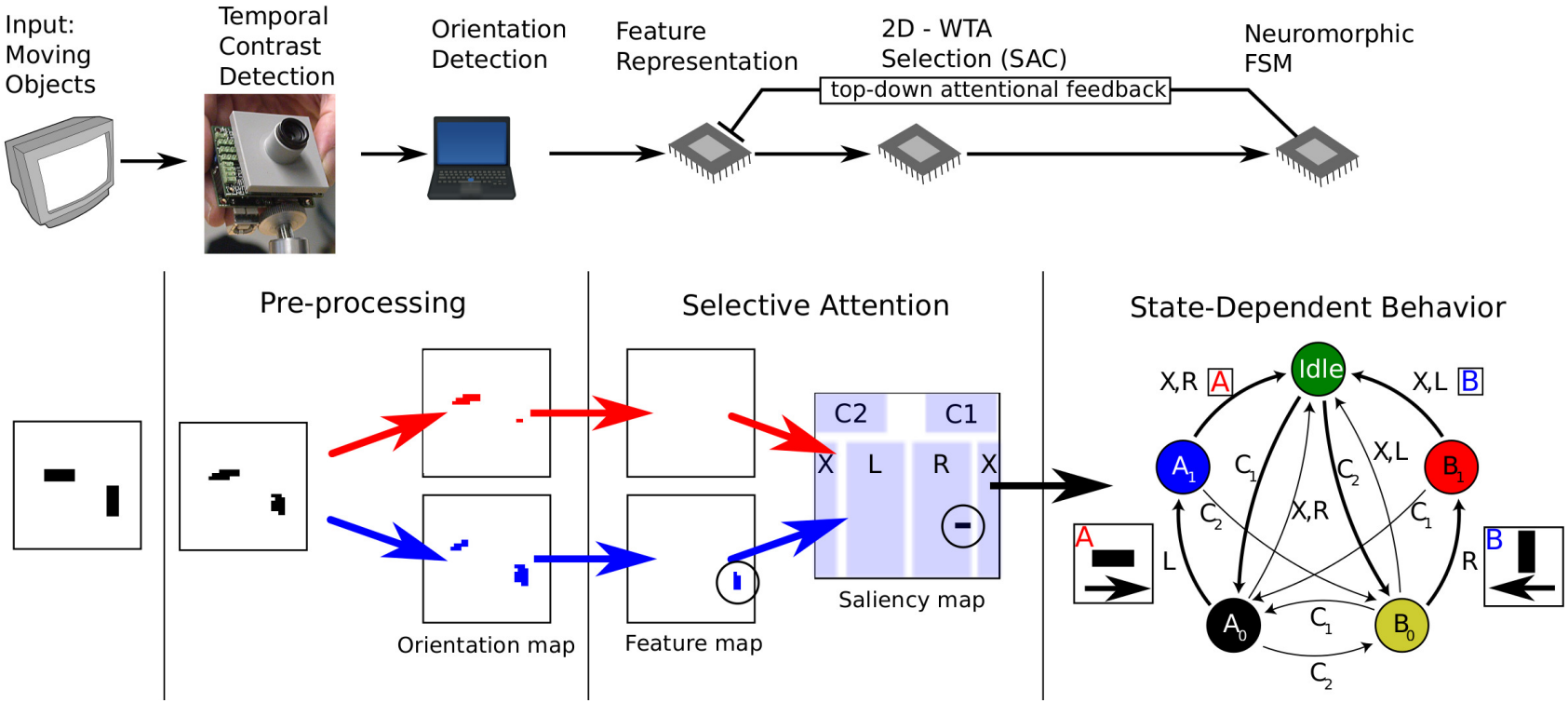
Synthesizing State-Dependent Behavior in Neuromorphic VLSI



(Neftci E., Binas J., Rutishauser U., Chicca E., Indiveri G., Douglas R., PNAS 2013)

(?, ?, ?)

Neuromorphic Setup Performing the Cognitive task



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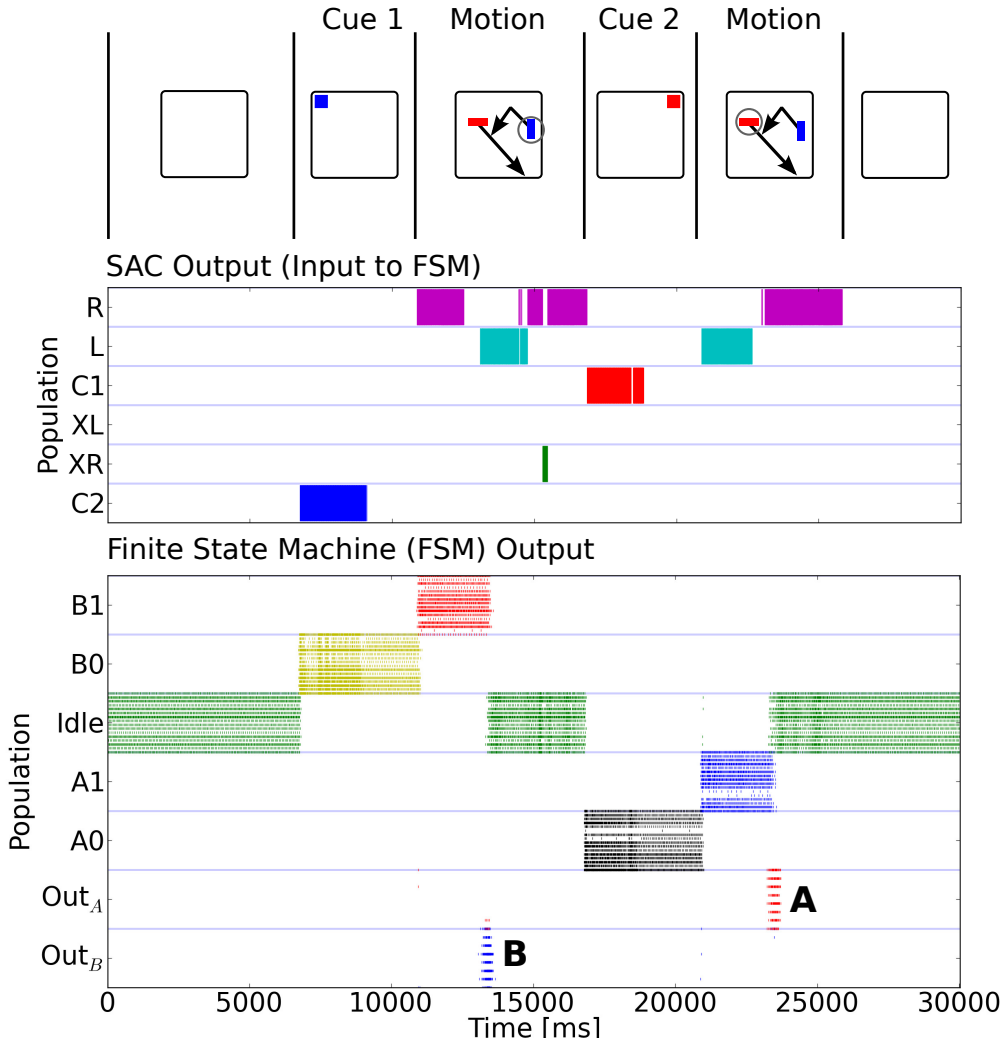
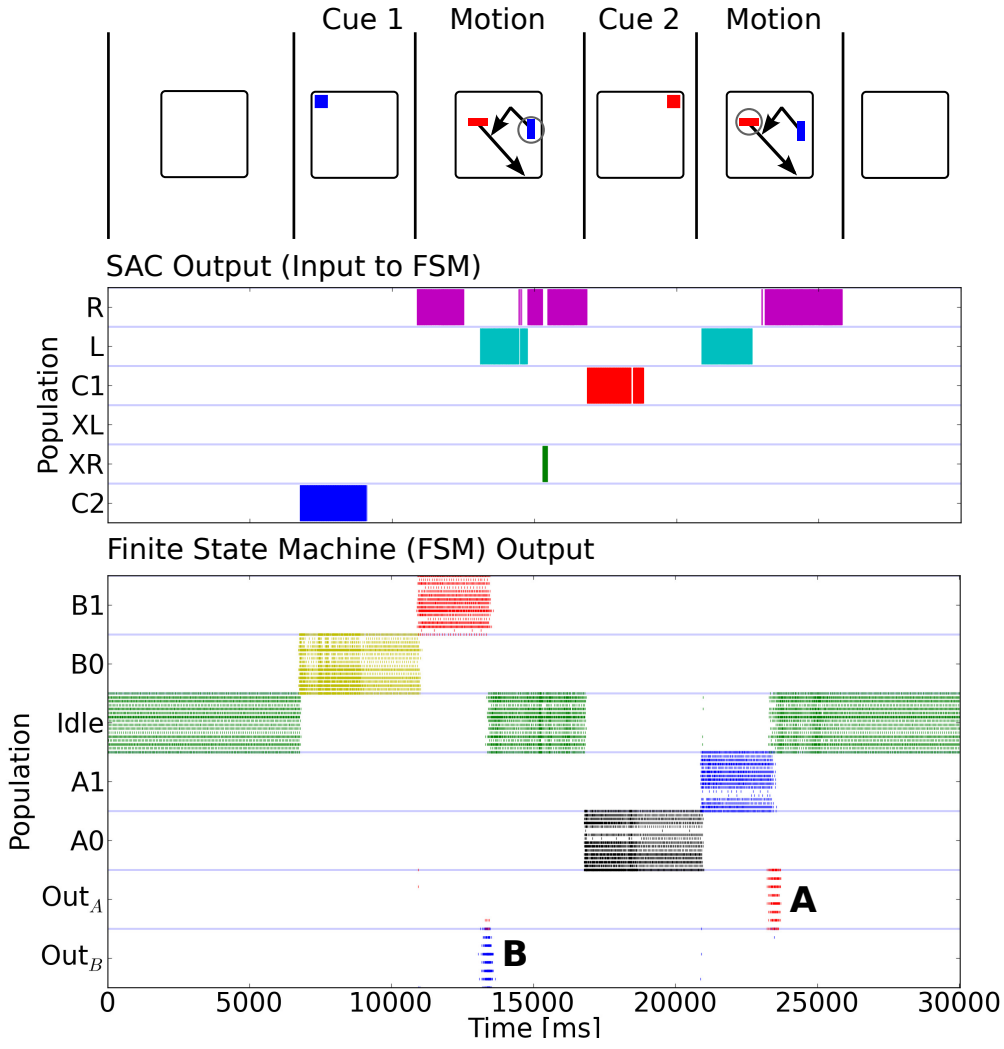


95% of state transitions were successful

(Neftci E., Binas J., Rutishauser U., Chicca E., Indiveri G., Douglas R., PNAS 2013)



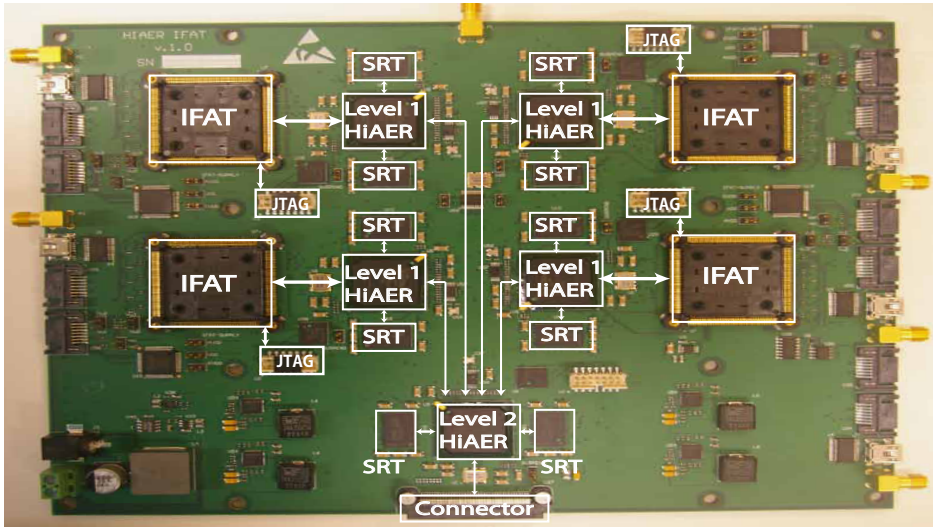
95% of state transitions were successful

(Neftci E., Binas J., Rutishauser U., Chicca E., Indiveri G., Douglas R., PNAS 2013)

Can it learn?

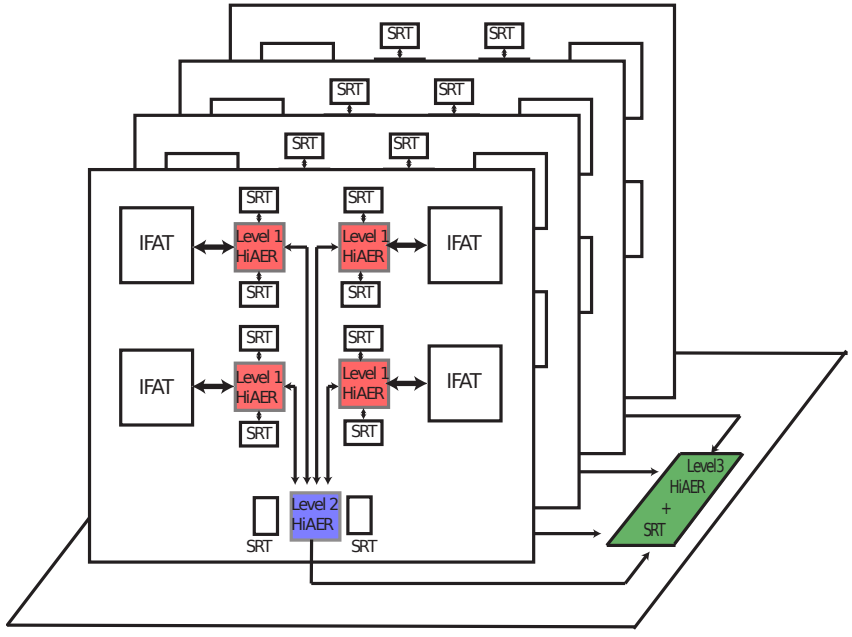
Can we extend this to a probabilistic representation?

Scalable event-based reconfigurable neuromorphic systems



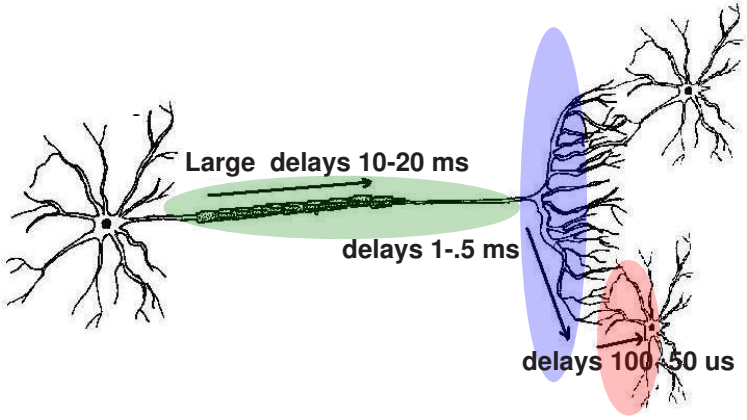
Hierarchical AER I&F Array Transceiver (HiAER IFAT)

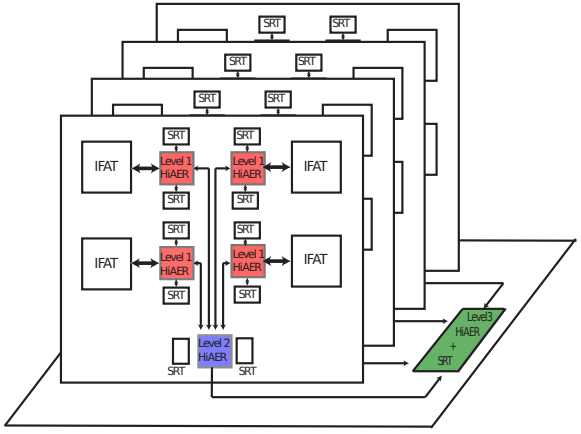
- $0.13\ \mu$m CMOS, $25\ \text{mm}^2$
- 65k dual-compartment conductance-based I&F neurons
- 65M synapses conductance-based dynamical synapses
- Reconfigurable, hierarchical AER interconnectivity

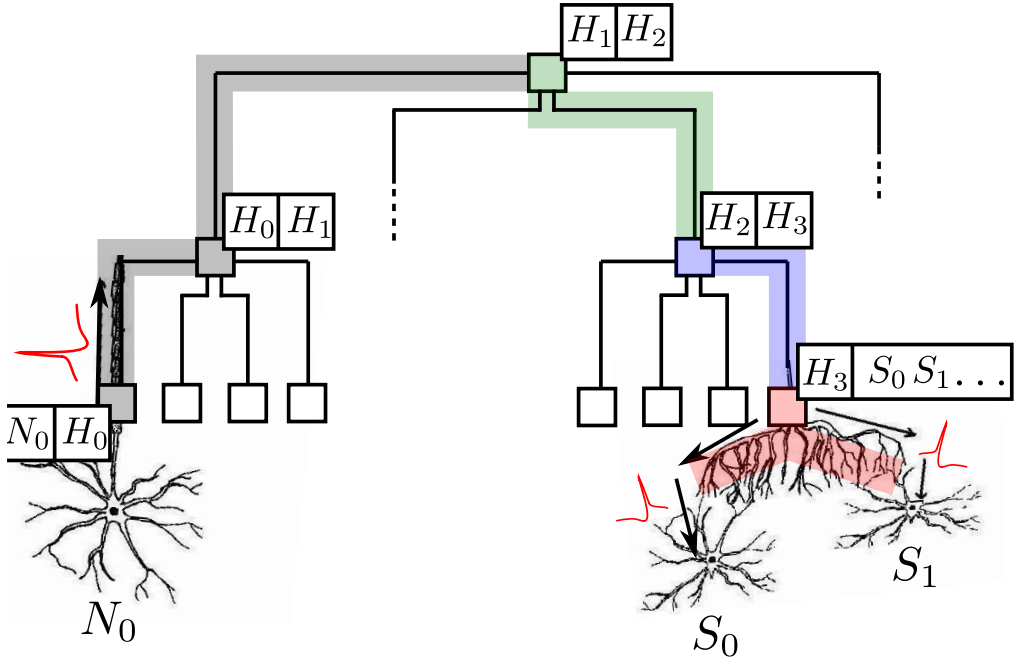


(T. Yu, S. Joshi, J. Park, S. Das, E. Neftci, C. Maier, G. Cauwenberghs)

Scalable Event Routing with Hierarchical AER

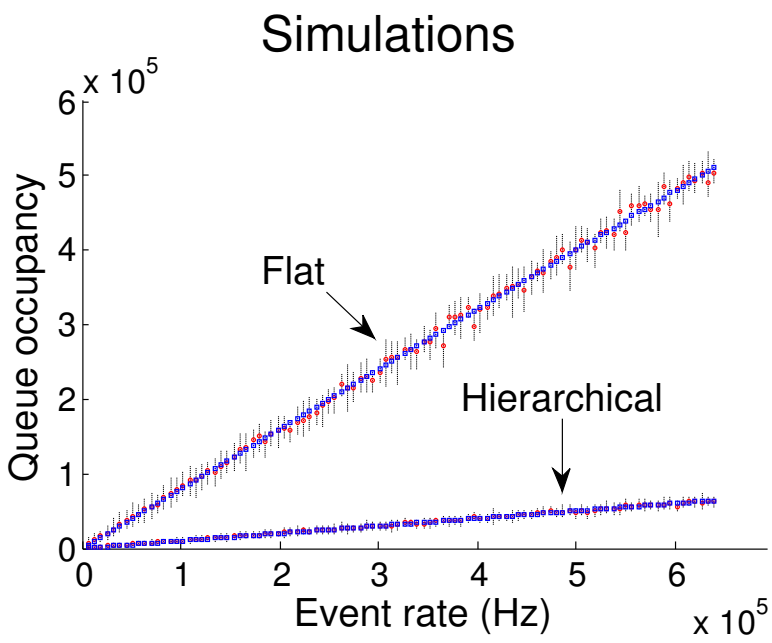






- Scalable, locally dense and globally sparse interconnectivity
- Simplifies the implementation of delays, deadlock-free

Latency Analysis



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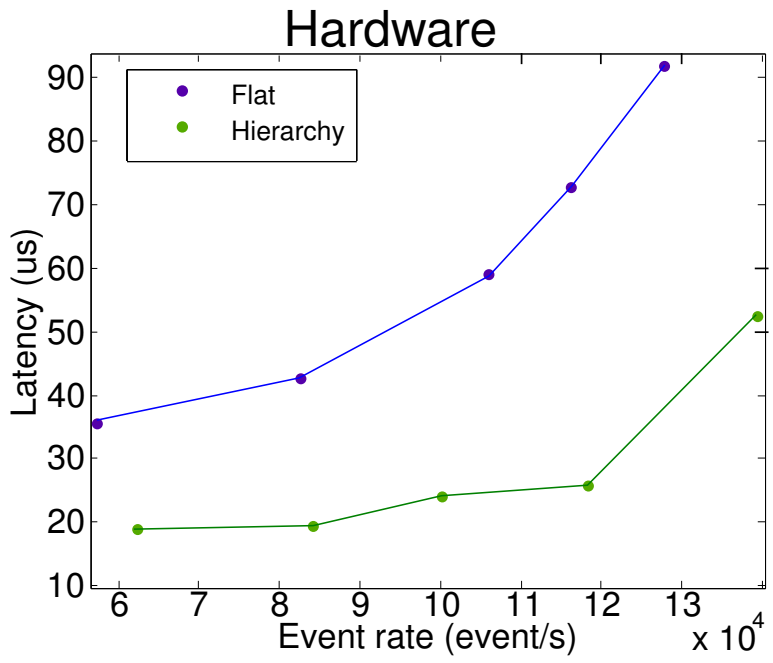
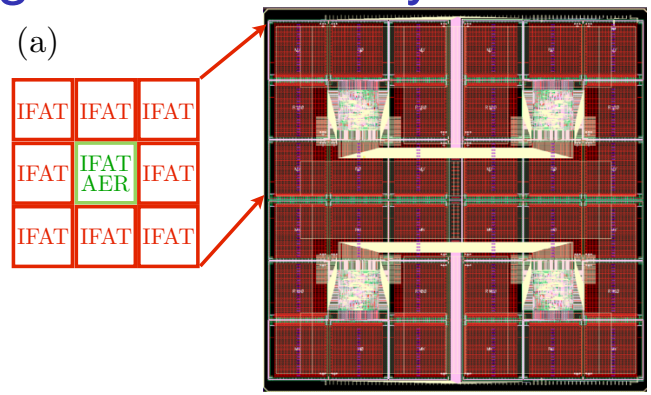
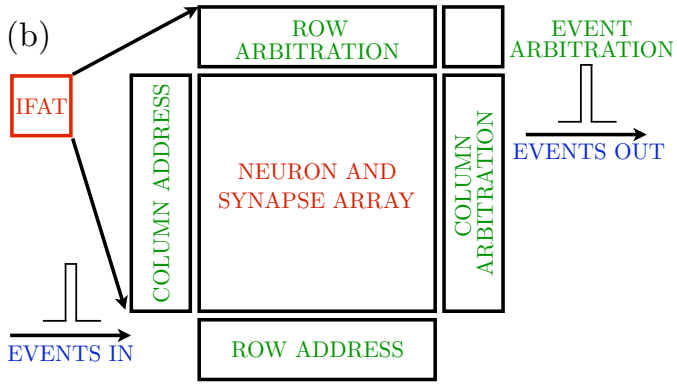
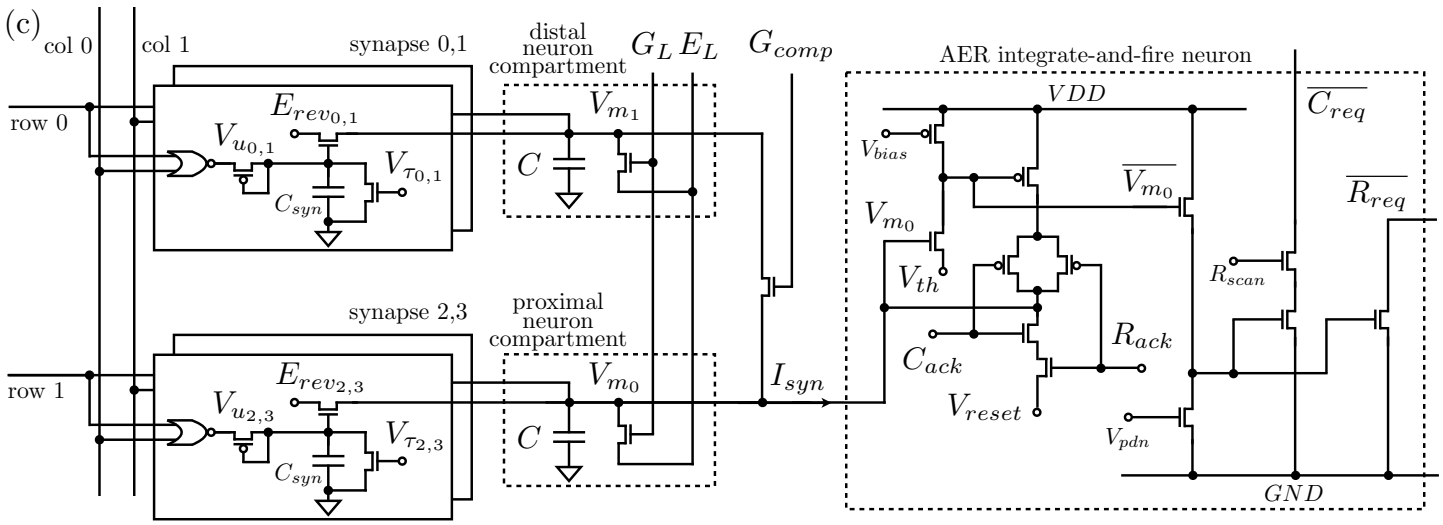


(Park, Yu, Maier, Joshi, & Cauwenberghs)

Integrate&Fire Array Transceiver (IFAT)



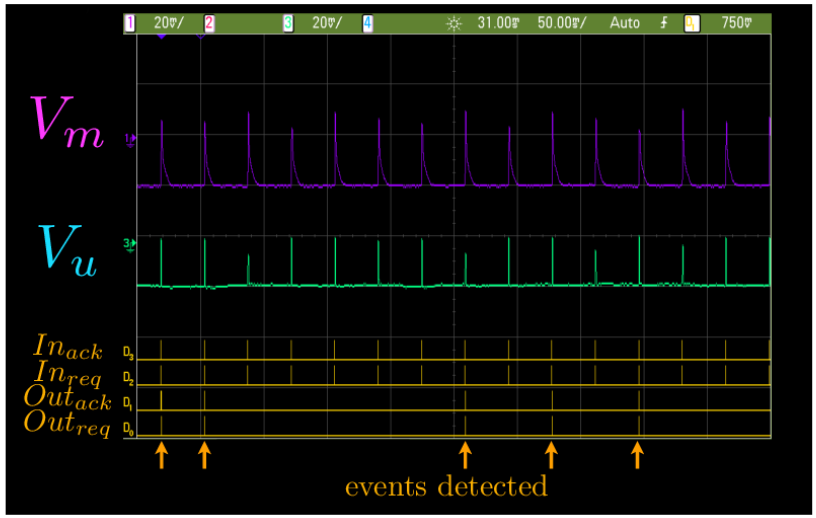


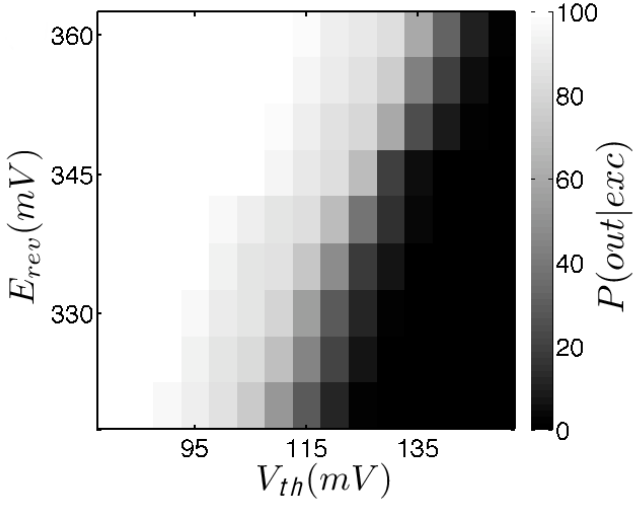


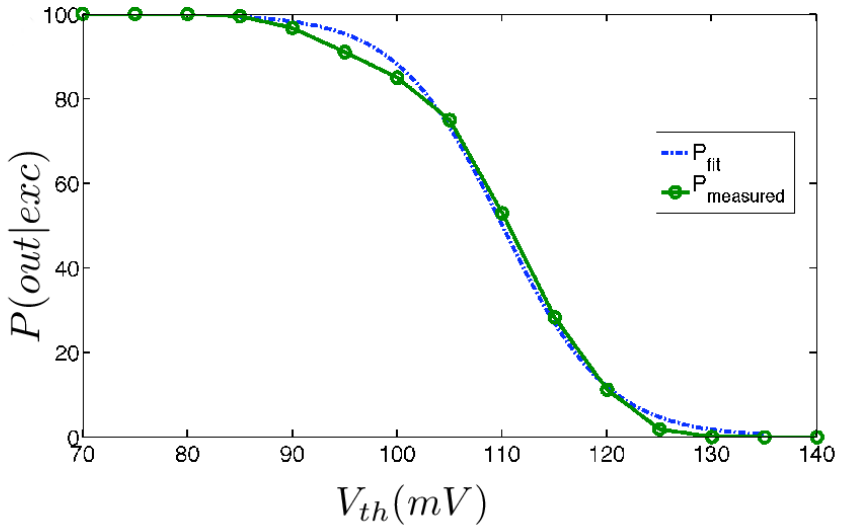
$$C_{m_n}\frac{dV_{i_n}}{dt} = I_{fb,i}\delta_0^n + \sum_j g_{syn(i,j)}\left(E^*_{rev} - V^*_{m_n}\right)$$
$$+g_{L_{i_n}}\left(E^*_{L_{i_n}} - V^*_{m_n}\right)$$
$$+g_{comp_{i_n}}\left(V^*_{m_1} - V^*_{m_0}\right)(-1)^n$$

(?, ?)

Probabilistic Neuron Activation







$$P(out|exc) = (1 + \exp(-V_{gs}/U_T))^{-1}$$

(?, ?)

Summary

Computation

A “cognitive” task specified as a state machine (MDP)

Algorithm

Winner-take-alls, Neural sampling

Hierarchical Communication Architecture (HIAER)

Implementation

Noisy and heterogenous VLSI spiking neurons

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- Abstract computational model constrains dynamics and # of free parameters

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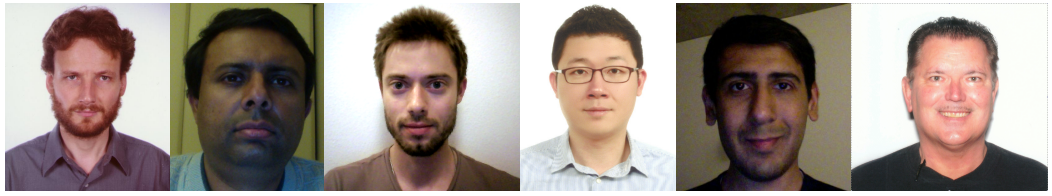
Implementation

Noisy and heterogenous VLSI spiking neurons

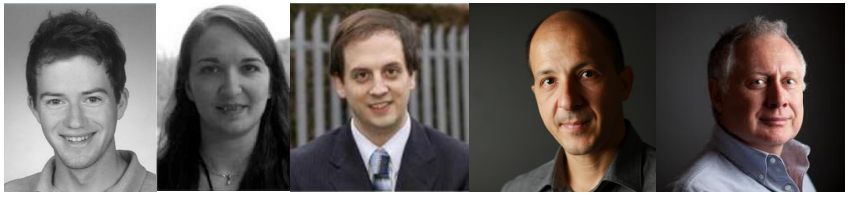
- Hierarchical architecture: locally dense globally sparse, programmable delays
- Abstract computational model constrains dynamics and # of free parameters
- Configuration, experimentation of neuromorphic chips with the python library pyNCS

`http://inincs.github.com/pyNCS/`

UCSD: Gert Cauwenberghs, Srinjoy Das, Bruno Pedroni, Jongkil Park, Siddarth Joshi, Ken Kreutz-Delgado



INI, UZH: Jonathan Binas, Elisabetta Chicca, Ueli Rutishauser, Giacomo Indiveri, and Rodney Douglas



Support: EU ICT Grant “SCANDLE” (231168), Swiss National Science Foundation, “Advanced Researchers” Grant (PA00P2_142058).

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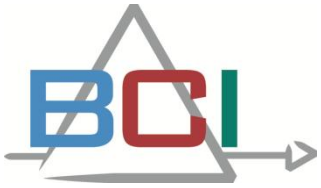

UC San Diego

Dynamics of Multifunction Brain Networks

Neuromorphic Engineering Winter School

January 8-10, 2014
UCSD, La Jolla, California

Organizers: Henry Abarbanel, Gert Cauwenberghs, Emre Neftci

Douglas, R., & Martin, K. (2007). Recurrent neuronal circuits in the neocortex. *Current Biology*, *17*(13), R496–R500.

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neural spiking, bursting, and excitability dynamics in reconfigurable analog VLSI. *Biomedical Circuits and Systems, IEEE Transactions on*. (in press)