

Philippe COUSSY

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Nationality: French

RESEARCH INTERESTS

High-Level Synthesis, ESL design, virtual prototyping, Computer Aided Design for SoC, Embedded Systems, Low-Power Design for FPGAs, Parallel Interleaver Architecture Design.

TEACHING INTERESTS

Undergraduate: Operating systems, Computer Architecture, Programming

Graduate: High-Level Synthesis, System-On-Chip Design, Computer-Aided Design

PROFESSIONAL EXPERIENCE

2004 - present

Associate Professor

Université de Bretagne-Sud UBS Lorient,
Science and Technique Department
Université Européenne de Bretagne UEB
Laboratoire CNRS Lab-STICC UMR3192

2003 - 2004

Assistant Professor

Université de Bretagne-Sud UBS Lorient,

2000 - 2003

Ph.D. Student & Teaching Assistant

Université de Bretagne-Sud UBS Lorient,

TEACHING EXPERIENCE

Undergraduate

IFI 1501 : Computer engineering I
ARS 1501 : Computer architecture I
IFI 1502 : Computer engineering II
ASA 1102 : Image processing

Graduate:

GIF 2105 : Computer engineering III
ARR 2202 : Computer architecture II
ARC 2301 : Advanced VLSI architecture

EDUCATION

Ph.D. in Electrical and Computer Engineering with honors, Dec. 2003

Université de Bretagne-Sud UBS

Lorient, 56, France,

Dissertation: "Interface and communication synthesis for IP core"

Advisor: Dr. Eric Martin (UBS/LESTER)

M.Sc. in Computer Science, Sept. 1999

Université Pierre et Marie Curie / Paris 6

Paris, 75, France,

Dissertation: "Software/Hardware co-design for a multiprocessor-based MPEG2 codec"

Advisor: Dr. J.L Danger, L. Naviner (ENST Paris/COmElec)

Certificate in VLSI and system design

M.A. in Computer Science, Jun. 1998

Université Pierre et Marie Curie / Paris 6

Paris, 75, France,

Dissertation: "Specification & design of a PI-BUS controller for embedded systems"

Advisor: Pr. A. Greiner, Dr. F. Petrot, D. Hommais (UPMC/LIP6)

Certificate in VLSI and system design

UNIVERSITY SERVICE

2004 – present

Responsible for the Bachelor degree in Electrical and Computer Engineering

2009 – 2012

Member of the Scientific Advisory Board of the Université de Bretagne-Sud

2009 – 2012

Member of the Advisory Board of the Lab-STICC

2001 – 2003

Member of the Advisory Board of the Doctoral School

AWARDS AND HONORS

PEDR (Prime d'Encadrement et de Recherche) Award,

Université de Bretagne-Sud (2008 – 2012)

PRIRE (Programme de Recherche Régional et Européen) Grant,

Region Bretagne (2005)

Outstanding Thesis Award,

Université de Bretagne-Sud (2003)

MESR (Ministère de l'Enseignement Supérieur et de la Recherche) Fellowship,

Université de Bretagne-Sud (2000 – 2003)

STUDENTS

Current Ph.D. Students

- Awais Hussain SANI,
Algorithm / Architecture Matching for the design of complex memory pattern-access for Digital Signal Processing applications
- Ghizlane LE BRETON-LHAIRECH,
High-Level Synthesis for low-power design on FPGA
- Kods TRABELSI,
Optimization methods for the hardware design of digital systems

Ph.D. Graduates

- Caaliph ANDRIAMISAINA,
High-Level Synthesis of multimode Architecture for DSP applications – 2008
Research Engineer at Université de Bretagne-Sud, Lorient.
- Cyrille CHAVET,
High-Level Synthesis of Space and Time Communication Adpater – 2007,
Associate Professor at Université de Bretagne-Sud, Lorient.
- Farhat THABET,
Behavioral Modeling for the Simulation and the High-Level Synthesis of Algorithmic IP Core – 2007
Research engineer at Commissariat à l'Énergie Atomique CEA-LIST

M.Sc. Graduates

- Aroua BRIKI
Hierarchical High-Level Synthesis: A Case study of a Reed Solomon Encoder-Decoder
Phd . Student at the Université de Bretagne-Sud (Lorient)
- Hicham LALAOUI HASSANI
Impact study of the HLS design steps and RTL coding styles on the design optimization – 2008
Phd . Student at UBS / IGA Morocco
- Mickael ADAM
Design Space Exploration for MPSoC – 2008
- Moahamed AABIDI
Design with HLS : A case study of a Maximum A Posteriori for Turbo decoder – 2008
- Ghizlane LE BRETON,
Bit-Width Aware High-Level Synthesis – 2007
PhD. Student at the Université de Bretagne-Sud (Lorient)
- Youcef MEKLA
High-Level Synthesis for Low-Power Design – 2006
Engineer at ACAMAS Electronique (Les Clayes sous Bois)
- Sebastien TREGAROT
Fast Prototyping of a MIMO application using the SocLib simulation platform – 2005
PhD. Student at the Université de Bretagne-Sud (Lorient) & Rubisoft company (Paris)
- Jean-Baptiste Le Goff,
Communication refinement for the simulation and the synthesis of algorithmic IP-core – 2004
Engineer at Atos Origin France (Rennes)

Ph.D. Jury Committee Member

- Caaliph ANDRIAMISAINA
- Fatma ABBES
- Cyrille CHAVET
- Farhat THABET

PATENTS

“ Method and device for interleaving data”, U.S. Patent application 20090031094, January 29, 2009
Cyrille Chavet, Philippe Coussy, Pascal Urard and Eric Martin,

“Procédé et dispositif d'entrelacement de données”, French Patent 0754793 10, April 30, 2008,
Cyrille Chavet, Philippe Coussy, Pascal Urard and Eric Martin

RESEARCH PROJECTS

"DGE Project: SoC toolKit for critical Embedded sysTems SoCKET",

Sponsor: Direction Générale des Entrprises DGE,

Industrial partners: Airbus, Astrium, CNES, STMicroelectronics, Thales R&T, Schneider Electric Industries, PSI-S, CEA-LETI, Magilem Design Services,

Academic partner: INPG-TIMA, UPS-IRIT, UBS-LabSTICC

2008 – 2011.

"Soclib Project: an open platform for virtual prototyping of multi-processors system on chip (MP-SoC) ",

Sponsor: Agence Nationale pour la Recherche ANR,

Industrial partners: STMicroelectronics, Thales Communication, Thomson R&D, Silicomp, Magilem Design Services, TurboConcept, CEA-LIST, CEA-LETI

Academic partner: CITI, Telecom Paris Tech, INRIA Futurs, IRISA, UPMC-LIP6, INPG-TIMA, LIS, LISIF, UBS-LabSTICC

2006 – 2009.

"ONAGRE Project: enviroNnement de coNception et de prototypAGed'applications Radio et mobile ",

Sponsor: France Telecom R&D,

Industrial partners: France Telecom R&D,

Academic partner: UBS-LabSTICC

2005 – 2008.

"SystemC'Mantic Project: an open platform for virtual prototyping of multi-processors system on chip (MP-SoC) ",

Sponsor: RNTL (Réseau National de recherche et d'innovation en Technologies logicielles),

Industrial partners: Thales Communication, CEA-LIST, Prosilog,

Academic partner: INPG-TIMA, UBS-LESTER

2003 – 2005.

"FLASH Project: Seed Optimisation and Indexing of Genomic Databases",

Sponsor: Actions de Recherche Coopérative ARC INRIA,

Partners: IRISA, LIFL, UBS-LESTER, INSERM U694

2006 – 2007.

"ALIPTA Project: Algorithmic Level IP for Telecom Applications ",

Sponsor: RNRT (Réseau National de Recherche en Télécommunications),

Industrial partners: Thales Communication, CEA-LIST, SACET, TNI-Valiosys, TurboConcept

Academic partner: ENST-Bretagne, UBS-LESTER

2002 – 2004.

PROFESSIONAL SERVICES

Editorship

Guest editor of the magazine *IEEE Design and Test of Computer, Special Issue on High-Level Synthesis*, July-August 2009

Editor of the book “*High-Level Synthesis: From Algorithm to Digital Circuit*”, P. Coussy and A. Morawiec, Springer, Berlin, Germany, 2008

Organizer

Organizer et Chair of the Tutorial on High-Level Synthesis, IEEE Design Automation Conference DAC San Francisco, USA, July 26-31, 2009

Co-organizer et Chair of the international workshop “ High-Level Synthesis: Next Step to Efficient ESL Design”, IEEE Asia and South Pacific Design Automation Conference ASP-DAC, Yokohama, Japan, January 19-22, 2009.

Co-organizer et Chair of the international workshop “ High-Level Synthesis: Back to the Future ”, IEEE Design Automation Conference DAC Anaheim, USA, June 8-13, 2008.

Co-organizer et Chair of the international workshop “The New Wave of the High-Level Synthesis ”, IEEE Design and Test in Europe DATE Munich, Germany, March 10-14, 2008.

Co-organizer et Chair of the 1st ECSI-UBS international High-Level Synthesis Workshop, (in conjunction with the Forum on Design Language FDL), Darmstadt, Germany, 2006 September 18.

Technical Program Committee

Co-Chair

IEEE Design and Test in Europe DATE, Topic D11 Architectural and High-Level Synthesis (2010)

Member

IEEE International Symposium on Circuits and Systems ISCAS (2005, 2006, 2007, 2008, 2009, 2010)

IEEE International Great Lake Symposium on VLSI GLSVLSI (2007, 2008, 2009)

French MANifestation des Jeunes Chercheurs STIC MajecSTIC (2006, 2007)

Reviewer

Journal

IEEE Design and Test of Computers

IEEE Transactions on Computer Aided-Design of Integrated Circuits and Systems (TCAD)

ACM Transactions on Embedded Computing System (ACM TECS)

Integration, the VLSI Journal, Elsevier Science

Journal of Embedded Computing (JEC)

International Journal of Circuits, Systems, and Computers (JCSC)

EURASIP Journal on Embedded Systems (JES)

Conference

IEEE Design Automation and Test in Europe (DATE)

IEEE International Symposium on Circuits and Systems (ISCAS)

IEEE International Great Lake Symposium on VLSI (GLSVLSI)

IEEE International Design Automation Conference (DAC)

MANifestation des Jeunes Chercheurs STIC (MajecSTIC 2006, 2007)

Journée Francophone sur l'Adéquation Algorithme/Architecture (JFAAA 2002)

Society membership

OSCI Member : Key Contributor in the Synthesis Working Group (SWG)
IEEE member (Institute of Electrical and Electronics Engineers, Inc.)
ECSI member (European Electronic Chips & Systems design Initiative 2006-2009)
Member of the CNRS Research Group on Information, Signal, Images and ViSion GdR-ISIS
Member of the CNRS Research Group on System-on-Chip & System-In-Package GdR SoC-SIP
EURASIP European Association for Signal Processing (2006-2008)

SOFTWARE RELEASES

GAUT

Open Source high-level synthesis tool
Automatic generation of an RTL architecture from a C/C++ specification
<http://lab-sticc.fr/www-gaut>
More than 100 downloads in 2007, 2008 and 2009 from more than 45 countries.

DsxPlore

Exploration and Rapid Prototyping of DSP Applications
SystemC behavioral simulation & High-Level Synthesis

STAR

Generation of space time adapters
Automatic synthesis of parallel interleaver architectures
IP-core integration

PUBLICATIONS

Book chapters

- GAUT: A High-Level Synthesis Tool for DSP applications,
P. Coussy, C. Chavet, P. Bomel, D. Heller, E. Senn, E. Martin,
“High-Level Synthesis: From Algorithm to Digital Circuits”, Springer, Berlin, Germany, 2008

Journals

- “An Introduction to High-Level Synthesis”,
P. Coussy, G. Gajski, A. Takach, M. Meredith
Special issue on High-Level Synthesis,
IEEE Design and Test of Computers, Vol. 26, Issue 4, July/August, 2009
- “Raising the Abstraction Level of Hardware Design”,
P. Coussy, A. Takach,
Special issue on High-Level Synthesis,
IEEE Design and Test of Computers, Vol. 26, Issue 4, July/August, 2009
- “Exploration and Rapid Prototyping of DSP Applications using SystemC Behavioral Simulation and High-Level Synthesis”,
F. Thabet, P. Coussy, D. Heller, E. Martin,
Journal of Signal Processing Systems, Issue 56, 2-3, September 2009
- “Multiple Word-Length High-Level Synthesis”,
P. Coussy, G. Le Breton, D. Heller
EURASIP Journal on Embedded Systems, July, 2008
- “Constrained algorithmic IP design for system-on-chip”,
P. Coussy, E. Casseau, P. Bomel, A. Baganne, E. Martin,
Integration, the VLSI Journal, Elsevier Science, Vol. 40, Issue 2, February 2007.
- “A Formal Method for Hardware IP Design and Integration under I/O and Timing Constraints”,
P. Coussy, E. Casseau, P. Bomel, A. Baganne, E. Martin,
ACM Transactions on Embedded Computing Systems vol 5, No. 1, pp. 29-53, 2006

International Conferences

- “VNS for High Level Synthesis”,
P. Coussy, A. Rossi, M. Sevaux, K. Sørensen, and K. Trabelsi..
In Proceedings of 8th Metaheuristics International Conference, MIC 2009, July 2009.
- “A Design Flow Dedicated to Multi-mode Architectures for DSP Applications”,
C. Chavet, C. Andriamisaina, P. Coussy, E. Casseau, E. Juin, P. Urard, E. Martin,
IEEE International Conference on Computer Aided Design, (ICCAD) 2007
- “Application of a design space exploration tool to enhance interleaver generation”,
C. Chavet, P. Coussy, P. Urard, E. Martin,
European Signal Processing Conference (EUSIPCO) 2007
- “Behavioral Description Model BDM for Design Space Exploration: a Case Study of His Algorithm for MC-CDMA System”,
F. Tabet, P. Coussy, D. Heller, E. Martin
European Signal Processing Conference (EUSIPCO) 2007
- “A Methodology for Efficient Space-Time Adapter Design Space Exploration: A Case Study of an Ultra Wide Band Interleaver”,
C. Chavet, P. Coussy, P. Urard, E. Martin,
IEEE International Symposium on Circuits and Systems ISCAS, 2007
- “Synthesis of Multimode digital signal processing systems”,
C. Andriamisaina, P. Coussy, E. Casseau
NASA/ESA Conference on Adaptive Hardware and Systems AHS, 2007
- “A Design Methodology for Space-Time Adapter”,
Chavet C., Coussy P., Urard P., Martin E.
ACM Great Lakes Symposium on VLSI - ACM Great Lakes Symposium on VLSI GLSVLSI, 2007
- “Design Space Exploration of DSP Applications Based on Behavioral Description Models”,
F. Tabet, P. Coussy, D. Heller, E. Martin
IEEE Workshop on Signal Processing Systems Design and Implementation SIPS, 2006
- “SystemC'mantic : A high level Modeling and Co-design Framework For Reconfigurable Real Time Systems”,
L. Kriaa, S. Adriano, E. Vaumorin, R. Nouacer, F. Blanc, S. Pajaniardja, P. Coussy, E. Martin, Heller D., Tabet F. et al
Forum on Design Languages FDL, 2005
- “A More Efficient and Flexible DSP Design Flow from MATLAB-SIMULINK”,
P. Coussy, G. Corre, P. Bomel, E. Senn, E. Martin
IEEE International Conference on Acoustic, Speech and Signal Processing ICASSP, 2005
- “High-level synthesis under I/O Timing and Memory constraints”,
P. Coussy, G. Corre, P. Bomel, E. Senn, E. Martin
IEEE International Symposium on Circuits And Systems ISCAS, 2005
- “A Methodoly for IP integration in DSP Soc: a case study of a MAP algorithm for turbo decoder”,
P. Coussy, D. Gnaëdig, A. Nafkha, A. Baganne, E. Boutillon, E. Martin
IEEE International Conference on Acoustics, Speech and Signal Processing ICASSP, 2004
- “IP integration methodology for SoC design”,
F. Abbes, E. Casseau, M. Abid, P. Coussy, J.-B. Legoff.
International Conference on Microelectronics ICM, 2004
- “A Methodoly for Timing and Structural Communication Refinement in DSP Systems”,
F. Thabet, J.-B. Legoff, P. Coussy, E. Martin
International Conference on Microelectronics ICM, 2004
- “Communication and Timing Constraints Analysis for IP Design and Integration”,
P. Coussy, A. Baganne, E. Martin,
IFIP WG 10.5 Very Large Scale Integration of System-on-Chip Conference VLSI-SOC, 2003

- “Virtual Component IP Re-use in Telecommunication Systems Design: A Case Study of MPEG-2 / JPEG2000 Encoder”,
P. Coussy, A. Baganne, E. Martin,
IEEE International Conference on Electronics, Circuits, and Systems ICECS, 2002
- “IP Cores Integration in DSP System-On-Chip Designs,”
P. Coussy, A. Baganne, E. Martin,
European Signal Processing Conference EUSIPCO, 2002
- “Platform-Based Design For Digital Signal Processing Systems: A Case Study of MPEG-2 / JPEG2000 Encoder”,
P. Coussy, A. Baganne, E. Martin,
IEEE International Conference on Communication Circuits and Systems ICCAS, 2002
- “A Design Methodology for IP Integration”,
P. Coussy, A. Baganne, E. Martin,
IEEE International Symposium on Circuits and Systems ISCAS, 2002.
- “A Design Methodology for Integrating IP into SOC Systems”,
P. Coussy, A. Baganne, E. Martin,
IEEE International Custom Integrated Circuits Conference CICC, 2002
- “A Methodology for Behavioral Virtual Component Specification Targeting SoC Design with High-Level Synthesis Tools”,
G. Savaton, P. Coussy, E. Casseau, E. Martin,
In Proc. of the Forum on Design Languages FDL, 2001
- “Design and synthesis of behavioral level virtual components”,
S. Pillement, O. Sentieys, D. Chillet, E. Casseau, P. Coussy, E. Martin, G. Savaton, S. Roux
IFIP WG 10.5 Very Large Scale Integration of System-on-Chip Conference VLSI-SOC, 2001.

National Conferences

- “Ordonnancement et Assignment en Synthèse de Haut Niveau”,
K. Trabelsi, P. Coussy, A. Rossi, M. Sevaux
9^{ème} congrès de la Société Française de Recherche Opérationnelle et d'Aide à la Décision ROADEF
February, 2008
- “Impact du type d'architecture sur la consommation d'une application”,
J. Laurent , P. Coussy
Journées Faible Tension Faible consommation - FTFC, May 21-23, 2007
- “Approche Automatique pour le Raffinement des Communications”,
F. Thabet, P. Coussy, E. Martin
Journées Francophones sur l'Adéquation Algorithme/Architecture JFAAA, 2005
- “Synthèse Comportementale Sous Contraintes de Communication et de Placement Mémoire pour les composants du TDSI”,
P. Coussy, G. Corre, P. Bomel, E. Senn, E. Martin
Colloque sur le Traitement du Signal et de l'Image GRETSI, 2005
- “Méthodologie de modélisation et d'implémentation d'adaptateurs spatio-temporels”,
C. Chavet, P. Coussy, P. Urard, E. Martin
MANifestation des Jeunes Chercheurs STIC MajecSTIC, 2005
- “Intégration Optimisée de Composants Virtuels orientés TDSI par la Synthèse d'Architecture”,
P. Coussy, A. Baganne, E. Martin, E. Casseau
Colloque sur le Traitement du Signal et de l'Image GRETSI, 2004
- “Réutilisation de Composant Virtuel dans les Systèmes de Télécommunication: Une Etude de Cas MPEG-2 / JPEG2000”,
P. Coussy, A. Baganne, E. Martin,
Journées Francophones sur l'Adéquation Algorithme/Architecture JFAAA, 2002.

- “Analyse Fonctionnelle des Moyens de communication Proposés dans les Systèmes sur Silicium”, P. Coussy, A. Baganne, E. Martin, Journées Francophones sur l'Adéquation Algorithme/Architecture JFAAA, 2002.

Others

Contributor to the following public documents

- “ESL Virtual System Design Modelling”, chapter V.2, European Electronic Design Automation Roadmap 2009, Medea+/Catrene, www.catrene.org
- “Esw and ESL to RTL design”, chapter V.3, European Electronic Design Automation Roadmap 2009, Medea+/Catrene, www.catrene.org

INVITED PRESENTATIONS (selected)

- “Multi-Mode Architecture Design with High-Level Synthesis”, Workshop on High-level synthesis, IEEE Design Automation and Test in Europe DATE, March 2008
- “GAUT: A High-Level Synthesis Tool”, Workshop on High-level synthesis ECSI Institute & UBS Workshop, September 18th, 2006
- “Conception d’architectures multi-mode pour les applications de traitement du signal” GDR Soc-Sip, thème Architecture et logiciel embarqué, March 18th, 2008
- “Panorama des techniques de synthèse de haut-niveau”, GDR Soc-Sip, thème Architecture et logiciel embarqué, February 19th, 2007

TOOL DEMONSTRATION / POSTER PRESENTATION (selected)

- Computer-Aided Network DEsign Workshop, October, 2009
- Workshop on High-Level Synthesis, IEEE Asia South Pacific Design Automation Conference ASP-DAC, January 2009
- Workshop on High-Level Synthesis, IEEE Design Automation Conference DAC, June 2008
- ACM-Sigda University Booth, IEEE Design Automation Conference DAC, June 2008
- Workshop on High-Level Synthesis, IEEE Design Automation Conference DAC, June 2008
- ACM-Sigda University Booth, IEEE Design Automation Conference DAC, June 2008
- Workshop on High-Level Synthesis, IEEE Design Automation and Test in Europe DATE, March 2008
- EDACentrum University Booth, IEEE Design Automation and Test in Europe DATE, March 2008
- Workshop on High-level synthesis ECSI Institute & UBS Workshop, 2006
- ACM-Sigda University Booth IEEE Design Automation and Test in Europe DATE, 2005
- PhD Forum of the IEEE International Conference on Design Automation and Test in Europe DATE, 2004