Philippe Coussy

Last name: COUSSY
First name: Philippe
Date of birth: 04 Sept. 1974
Maried, 1 child

Full Professor
Université de Bretagne-Sud
Lab-STICC, UMR CNRS 6285
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Education	**Habilitation to Lead Researches HDR (Sept. 2011)** **(Information and Communication Science and Technology)** Université de Bretagne-Sud – UBS / Lab-STICC (CNRS) Lorient, France Dissertation : "Architectural Synthesis for signal and image processing applications" **Ph.D. in Electrical and Computer Engineering with honors (Dec. 2003)** Université de Bretagne-Sud UBS / LESTER Lorient, France, Dissertation: "Interface and communication synthesis for IP core" Advisor: Pr. Eric Martin **M.Sc. in Computer Science (Sept. 1999)** Université Pierre et Marie Curie / Paris 6 Paris, France, Dissertation: "Software/Hardware co-design for a multiprocessor-based MPEG2 codec" Advisor: Dr. J.L Danger, L. Naviner (ENST Paris/COmElec) Certificate in VLSI and system design **M.A. in Computer Science (June 1998)** Université Pierre et Marie Curie / Paris 6 Paris, France, Dissertation: "Specification & design of a PI-BUS controller for embedded systems" Advisor: Pr. A. Greiner, Dr. F. Petrot (UPMC/LIP6) Certificate in VLSI and system design
Current and Previous Academic Positions	**Full Professor** Université de Bretagne Sud, Science and Technique Department Lab-STICC UMR6285, CNRS **Associate Professor - HDR** Université de Bretagne Sud, Science and Technique Department Lab-STICC UMR3192, CNRS **Assistant Professor (Sept. 2003 – Sept. 2004)** Université de Bretagne-Sud UBS Lorient LESTER Lab. **Ph.D. Student & Teaching Assistant (Sept. 2000 – Sept. 2003)** Université de Bretagne-Sud UBS Lorient,
Research interests	Computer Aided Design: High-Level Synthesis, Virtual prototyping, HW-SW co-design, Design space exploration, Hardware Architectures: Embedded Systems, Low-Power Design, MPSoC design, Parallel Interleaver Architecture Design, Neuromorphic and bio-inspired hardware architectures
Teaching interests	**Graduate:** High-Level Synthesis, System-On-Chip Design, Computer-Aided Design **Undergraduate:** Operating systems, Computer Architecture, Programming, Microcontroller
Awards and Honors	**PES** (Prime Excellence Scientifique- AAAA) Award (2012 – 2016) **PEDR** (Prime d'Encadrement et de Recherche) Award, (2008 – 2012) **PRIRE** (Programme de Recherche Régional et Européen) Grant, (2005) **Outstanding Thesis Award**, Université de Bretagne-Sud (2003) **MESR** (Ministère de l'Enseignement Supérieur et de la Recherche) Fellowship, (2000 – 2003)

University Services	**Member of the Advisory Board** of the Engineering Department of the Université de Bretagne-Sud (2012 – 2016) - Elected **Director** of the Bachelor degree in Electrical and Computer Engineering (2004 – 2012) **Member of the Scientific Advisory Board** of the Université de Bretagne-Sud (2009 – 2012) - Elected **Member of the Advisory Board** of the Lab-STICC (2009 – present) - Elected **Member of the Advisory Board** of the Doctoral School (2001 – 2003) - Elected
Professional Activities, Membership, and Services	**Editorship** **Co-editor** of the book "Advanced hardware design for error correcting codes" (Springer), 2014 **Associated Editor** of the IEEE Signal Processing Letters since April 2013 **Guest editor** for a special issue of Journal of Electrical and Computer Engineering on "ESL Design Methodology", 2012 **Guest editor** for a special issue of IEEE Design and Test of Computer on "High-Level Synthesis", 2009 **Co-editor** of the book "High-Level Synthesis: From Algorithm to Digital Circuit" (Springer) 2008 **Professional Society Membership and Leadership** **Member of the technical committee** of the IEEE Signal Processing Society, *Design and Implementation of Signal Processing Systems (DISPS)* (2011–today) **Member of the Technical Program Committee of the** French Agence Nationale de la Recherche ANR, 2012-2014 **Member of the Advisory Board** of the National Research Group on SoC-SIP (since Oct. 2011) **Topic Chair of « Embedded Software and Hardware architectures »** of the National Research Group on SoC-SIP (since Dec. 2011) **Member of the European Network of Excellence HiPEAC** (since Dec. 2009) **IEEE member** (since Sept. 2004) **ACM member** (since Sept. 2010) **OSCI Member**, Synthesis Working Group (SWG) (Key Contributor 2009, Affiliate member 2010) **Member of the CNRS Research Group** on Information, Signal, Images and ViSion GdR-ISIS (Since Sept. 2005) **Member of the CNRS Research Group** on System-on-Chip & System-In-Package GdR SoC-SIP (Since 2005) **EURASIP member** European Association for Signal Processing (2006-2008) **ECSI member** (2006-2009) **Service to Professional Conferences** ***Various chair positions*** General chair: ESLsyn 2012, Neucomp 2015 Program chair: Neucomp 2015-2013, HLS4HPC2013, ESLsyn 2011 Track chair: IEEE DATE 2010-2013 (chair/co-chair track HLS), IEEE GLS-VLSI 2014 Session chair: IEEE DATE 2010 to 2013, IEEE ICASSP 2011, IEEE ISCAS 2010 and 2005, IEEE GLSVLSI 2007 Tutorial chair: IEEE DAC 2010, IEEE DAC 2009 Workshop chair: Neucomp 2013, HLS4HPC2013, IEEE ASP-DAC 2009, IEEE DATE 2008, IEEE DAC 2008, FDL 2006 ***Technical Program Committee member*** **International:** IEEE DATE 2010-2015, IEEE SIES 2014-2015, IEEE ASAP 2011, 2014-2015, IEEE GLSVLSI 2007-2015, Neucomp 2013-2015, ESLsyn 2011-2012, IEEE FPL 2013-2015, IEEE ISCAS 2005-2013, 2015, IEEE SIPS 2011-2015, ERDIAP 2011 **National:** ComPAS 2014, SYMPA 2011-2012, Doctoriales 2002 ***Technical Review Committee member*** **International:** IEEE DAC 2005, 2012-2013, 2015, IEEE DATE 2010-2015, IEEE ICASSP 2011-2014, IEEE ASAP 2011-2015, IEEE FPL 2013-2015, IEEE SIPS 2011-2015, IEEE ICECS 2010, IEEE ISCAS 2005-2013, 2015, IEEE GLSVLSI 2007-2015, Reconfig 2011 **National:** ComPAS 2014, GRETSI 2011, 2013 SYMPA 2011, MajecSTIC 2006-2007, JFAAA 2002

	Journal Review IEEE Design and Test of Computers, IEEE Transactions on Computer Aided-Design of Integrated Circuits and Systems (TCAD), IEEE Journal on Emerging and Selected Topics in Circuits and Systems (JETCAS), IEEE Transactions on Signal Processing (TSP), ACM Transactions on Design Automation of Electronic System (TODAES), ACM Transactions on Embedded Computing System (TECS), Integration, the VLSI Journal - Elsevier Science, Journal of Embedded Computing (JEC), International Journal of Circuits, Systems, and Computers (JCSC), Journal on Embedded Systems, EURASIP (JES), Embedded Hardware Design (Microprocessors and Microsystems MICPRO) – Elsevier, Microelectronics Journal – Elsevier **Tutorial/Workshop organizer (at)** HiPEAC 2013, IEEE DATE 2013, IEEE CODES-ISSS 2010, IEEE DAC 2010-2009, IEEE ASP-DAC 2009, IEEE DAC 2008, IEEE DATE 2008, FDL 2006 **Proposal Review** **External proposal reviewer,** Natural Sciences and Engineering, Research Council of Canada, 2011, 2012, 2014, 2015 **External proposal reviewer,** Israel Science Foundation**,** 2013 **External proposal reviewer,** Foundation for Science and Technology Portugal 2012 **External proposal reviewer,** French Agence Nationale de la Recherche ANR, Topic « Ingénierie Numérique & Sécurité » - INS 2011-2013 **External proposal reviewer,** French Agence Nationale de la Recherche ANR, 2014 **Contributor to the following public documents** "ESL Virtual System Design Modelling", chapter V.2, European Electronic Design Automation Roadmap 2009, Medea+/Catrene, www.catrene.org "Esw and ESL to RTL design", chapter V.3, European Electronic Design Automation Roadmap 2009, Medea+/Catrene, www.catrene.org
EDA Software Releases	**GAUT** Open Source high-level synthesis tool Automatic generation of an RTL architecture from a C/C++ specification http://lab-sticc.fr/www-gaut More than 100-150 downloads/year since 2007from more than 60 countries. **DsxPlore** Exploration and Rapid Prototyping of DSP Applications SystemC behavioral simulation & High-Level Synthesis **STAR** Generation of space time adapters Automatic synthesis of parallel interleaver architectures IP-core integration
Student Advising	**Current Ph.D. Students** **Robin Danilo** Bio-inspired vision system based on binary sparse neural networks **Huges Wouafo** Neuromorphic hardware architectures and sparse neural coding **Satyajit Das** Architecture and programming model support for reconfigurable accelerators in shared-memory many-cores **Ph.D. Graduates** **Thomas Peyret** High-Level Synthesis for designing fault tolerant architectures on FPGA, **Mohamed Ben Hamouda** High level synthesis for circuit generation that supports software like debugging **Saeed Ur Remhan** Toward Flexible Hardware Architectures for Parallel Turbo-like Decoders. **Paolo Burgio** Use of shared memory in the context of embedded multi-core processor: exploration of the technology and its limits **Aroua Briki** Architectural Synthesis for designing complex memory unit

	Awais Sani, Algorithm / Architecture Matching for the design of complex memory pattern-access for Digital Signal Processing applications **Ghizlane Lebreton-Lhairech,** High-Level Synthesis for low-power design on FPGA **Kods Trabelsi,** Optimization methods for the hardware design of digital systems **Caaliph Andriamisaina,** High-Level Synthesis of multimode Architecture for DSP applications **Cyrille Chavet,** High-Level Synthesis of Space and Time Communication Adpater **Farhat Thabet** Behavioral Modeling for the Simulation and the High-Level Synthesis of Algorithmic IP Core **<u>M.Sc. Graduates</u>** **Baptiste Goupille-Lescar** Design and programmation of reconfigurable accelerators in shared-memory many-cores **Sureshbabu Ramesh** Study and analysis of application mapping methods on CGRAs **Robin Danilo** Architecture and Programming Model Support for Efficient Heterogeneous Computing on Tigthly-Coupled Shared-Memory Clusters **Nicolas Charpentier** Neuromorphic hardware architectures and sparse neural coding **Hugues Wouafo** HLS tool based on LLVM front-end **Michelle Furtado Pinheiro Do Carmo** Virtual prototyping of an MP3 codec with the SocLib platform **Vianney Lapotre** Branch prediction for high-level synthesis **Aroua briki** Hierarchical High-Level Synthesis: A Case study of a Reed Solomon Encoder-Decoder **Hicham Lalaoui Hassani** Impact study of the HLS design steps and RTL coding styles on the design optimization **Mickael Adam** Design Space Exploration for MPSoC **Moahamed Aabidi** Design with HLS : A case study of a Maximum A Posteriori for Turbo decoder **Ghizlane LeBreton,** Bit-Width Aware High-Level Synthesis **Youcef Mekla** High-Level Synthesis for Low-Power Design **Sebastien Tregarot** Fast Prototyping of a MIMO application using the SocLib simulation platform **Jean-Baptiste Le Goff,** Communication refinement for the simulation and the synthesis of algorithmic IP-core **<u>Post-doc researchers</u>** **Awais Sani** Auto-configurable Hardware Architectures for Parallel Turbo-like Decoders **Jorgiano Vidal** HLS tool front-end **Caaliph Andriamisaina** Automatic generation of simulation model using HLS **<u>Engineers</u>** **Mickael Lanoe** GAUT3 : High-Level Synthesis tool **LinFeng Ye** Parallel interleaver generator
Research Projects	**SPICA** 2015-2019, FUI Project, STMicroelectronics, Dolphin, TIMA, Lab-STICC **SENSE** 2013-2016, Brittany county, *Lab-STICC (UBS, Telecom Bretagne), IRISA* **Astrium ST-2** 2013, Private contract, *Lab-STICC, Astrium* Space Transportation

	MPPA	2013, Private contract, *Lab-STICC,* Kalray
	GIGADEC	2011-2013, Brittany county, Lab-STICC (UBS, Telecom Bretagne), Turbo-concept
	Astrium ST	2011/2012, Private contract, *Lab-STICC, Astrium* Space Transportation
	Projet P	2011-2013, FUI project, *Aboard Engineering, AGC Solutions, AdaCore, Airbus, Altair, ASTRIUM, ATOS Origin, Continental, Ecole des Ponts ParisTech, INRIA/Aoste-Espresso-Metalau, IRIT/INPT/ENSEEIHT, Lab-STICC, ONERA, Rockwell Collins, Sagem Défense Sécurité, Scilab, ST Informatique Services, Thales Alenia Space, Thales Avionics*
	SoCKET	2008 – 2011, FUI project, *Airbus, Astrium, CNES, STMicroelectronics, Thales R&T, Schneider Electric Industries, PSI-S, CEA-LETI, Magilem Design Services, INPG-TIMA, UPS-IRIT, UBS-LabSTICC*
	SocLib	2006-2009, ANR/RNTL platform, *STMicroelectronics, Thales Communications, Thomson Silicon Components, Prosilog, TurboConcept, Silicomp, UPMC/LIP6, ENST, UPMC/LISIF, CEA LIST, INRIA Futurs, IRISA, LESTER/Lab-STICC, IETR INSA, TIMA, CEA LIST, CITI*
	FLASH	2006-2007, ARC INRIA, *IRISA, LIFL, LESTER, INSERM U694*
	Onagre	2005-2008, CRE France Telecom, *France Telecom, LESTER/Lab-STICC*
	ANTELOP	2005, PRIRE, *Lab-STICC*
	SystemC'Mantic	2003-2005, RNTL project, *Thales communications, TIMA, CEA LIST, TIMA, LESTER*
	ALIPTA	2002-2004, RNRT project, *Valiosys, Thales, Sacet, Turbo-Concept, ENST Bretagne*
Patents	« Architecture de réseau de neurone, procédé d'obtention et programmes correspondants », FR1261155 / R21609WO, December 2012 « Système de traitement de données avec cache active », FR1256715, june 2012 « Dispositif auto-configurable d'entrelacement / désentrelacement de trames de données», FR1251688. February. 2012 "Self-configurable device for interleaving/de-interleaving data frames**"** WO2013124449 A1, August 2013 "Apparatus for data interleaving algorithm", CNRS – STMicroelectronics U.S. Patent application 20090031094, January 29, 2009. « Procédé et dispositif d'entrelacement de données », CNRS – STMicroelectronics, Brevet Français n° 0754793 10, 30 April 2007.	
Technology transfer	GAUT: High-Level Synthesis /System synthesis on FPGA: On-going creation of a start up with SATT Grand Ouest support GRAAL: Architecture for on line memory mapping and conflict free parallel interleaver design	
Publications	***Journal papers*** P. Coussy; C. Chavet, H. Nono Wouafo, L. Conde-Canencia "**Fully-Binary Neural Network Model and Optimized Hardware Architectures for Associative Memories**", *ACM Transactions on Journal of Emerging Technologies, Special issue on Neuromorphic and Brain-Inspired Computing Systems* (under review, major revisions) A. Sani, P. Coussy, C. Chavet, "**A First Step Toward On-Chip Memory Mapping for Parallel Turbo and LDPC Decoders: A Polynomial Time Mapping Algorithm",** *IEEE Transactions on Signal Processing.* Vol. 61, Number 16, pp. 4127-4140, August 2013 V. Lapôtre, P. Coussy, C. Chavet: "**Introduction de la prédiction de branchement dans la synthèse de haut niveau".** *Technique et Science Informatiques*, Vol. 32, Issue 2, pp. 281-301 2013 C. Andriamisaina, P. Coussy, E. Casseau, C. Chavet, **"High-Level Synthesis for Designing Multi-mode Architectures"**, *IEEE Transactions on Computer Aided Design of Integrated Circuits and Systems (TCAD)*, Vol. 29, Issue 11, pp. 1736-1749, November 2010. P. Coussy, A. Takach, **"Raising the Abstraction Level of Hardware Design"**, *Special issue on High-Level Synthesis, IEEE Design and Test of Computers*, Vol. 26, Issue 4, July/August, 2009. P. Coussy, G. Gajski, A. Takach, M. Meredith, **"An Introduction to High-Level Synthesis"**, *Special issue on High-Level Synthesis, IEEE Design and Test of Computers*, Vol. 26, Issue 4, July/August, 2009. F. Thabet, P. Coussy, D. Heller, E. Martin, **"Exploration and Rapid Prototyping of DSP**	

Applications using SystemC Behavioral Simulation and High-Level Synthesis", *Journal of Signal Processing Systems, Springer*, Issue 56, 2-3, September 2009.
P. Coussy, G. Le Breton, D. Heller, **"Multiple Word-Length High-Level Synthesis"**, *EURASIP Journal on Embedded Systems*, July, 2008.

P. Coussy, E. Casseau , P. Bomel, A. Baganne, E. Martin, **"Constrained algorithmic IP design for system-on-chip"**, *Integration, the VLSI Journal, Elsevier Science*, Vol. 40, Issue 2, February 2007.

P. Coussy, E. Casseau, P. Bomel, A. Baganne, E. Martin, **"A Formal Method for Hardware IP Design and Integration under I/O and Timing Constraints"**, *ACM Transactions on Embedded Computing Systems,* Vol 5, No. 1, pp. 29-53, 2006.

Book chapters

P. Coussy, C. Chavet, **"Hardware Design of Parallel Interleaver Architectures: A Survey"**, to appear in *"Advanced hardware design for error correcting codes", Springer, Berlin, Germany*, 2014.

P. Coussy, C. Chavet, P. Bomel, D. Heller, E. Senn, E. Martin, "**GAUT: A High-Level Synthesis Tool for DSP applications"**, *"High-Level Synthesis: From Algorithm to Digital Circuits", Springer, Berlin, Germany*, 2008.

K. Trabelsi, M. Sevaux, P. Coussy, A. Rossi, K. Sörensen, **"Advanced Metaheuristics for High-Level Synthesis"**, *In Metaheuristics. Springer*, 2010.

International Conferences

S. Rehman, C. Chavet, P. Coussy, A. Sani, "**In-place memory mapping approach for optimized parallel hardware interleaver architectures**", , *IEEE International Conference on Design, Automation and Test in Europe (DATE) 2015*
H. Nono Wouafo, C. Chavet and P. Coussy, "**Improving Storage of Patterns in Recurrent Neural Networks: Clones Based Model and Architecture**", IEEE International Symposium on Circuits and Systems (ISCAS), 2015.
R. Danilo, V. Gripon, L. Conde-Canencia, P. Coussy, "**Algorithm and Implementation of an Associative Memory for Oriented Edge Detection Using Improved Clustered Neural Networks**", *IEEE International Symposium on Circuits and Systems (ISCAS),* 2015.
R. Danilo, V. Gripon, L. Conde-Canencia, P. Coussy, W. Gross, "**Restricted Clustered Neural Network for Storing Real Data**",*ACM Great Lakes Symposium on VLSI on VLSI (GLSVLSI)* 2015.
T. Peyret, G. Corre, M. Thevenin, K. Martin, P. Coussy, "**Efficient application mapping on CGRAs based on backward simultaneous scheduling/binding and dynamic graph transformations"**. IEEE *International Conference on Application-specific Systems, Architectures and Processors (ASAP),* 2014
P. Burgio, R. Danilo, A. Marongiu, P. Coussy, L. Benini, "**A HLS-Based Toolflow to Design Next-Generation Heterogeneous Many-Core Platforms with Shared Memory**". EUC 2014: 130-137
P. Burgio, R. Danilo, A. Marongiu, P. Coussy, L. Benini, "**A tightly-coupled Hardware Controller to improve scalability and programmability of shared-memory heterogeneous clusters**", *IEEE International Conference on Design, Automation and Test in Europe (DATE) 2014*

S. Reehman, C. Chavet, P. Coussy, "**A memory mapping approach based on network customization to design conflict-free parallel hardware architectures**". ACM Great Lakes Symposium on VLSI 2014: 193-198

T. Peyret, G. Corre, M. Thevenin, K. Martin, P. Coussy, "**An automated design approach to map applications on CGRAs**", ACM Great Lakes Symposium on VLSI 2014: 229-230

M. Ben Hammouda, P. Coussy, L. Lagadec, "**A design approach to automatically generate on-chip monitors during high-level synthesis of hardware accelerator**", ACM Great Lakes Symposium on VLSI 2014: 273-278

S. Rehman, A. Sani, C. Chavet, P. Coussy, "**Embedding polynomial time memory mapping and routing algorithms on-chip to design configurable decoder architectures**", *IEEE International Conference on Acoustics, Speech and Signal Processing (ICASSP)*, 2014

M. Ben Hammouda, P. Coussy, L. Lagadec, "**A design approach to automatically**

synthesize ANSI-C assertions during High-Level Synthesis of hardware accelerators", *IEEE International Symposium on Circuits and Systems (ISCAS)*, 2014

A. Briki, C. Chavet, P. Coussy, "**A Conflict-Free Memory Mapping Approach to Design Parallel Hardware Interleaver Architectures with Optimized Network and Controller"**, *IEEE Workshop on Signal Processing Systems (SIPS)* 2013.

V. Lapotre, P. Coussy, C. Chavet, H. Wouafo and R. Danilo, **"Dynamic Branch Prediction For High-Level Synthesis"**, *IEEE International Conference on Field Programmable Logic and Applications (FPL)* 2013

S. Ur Rehman, A. Sani, P. Coussy, C. Chavet, **"On-Chip Implementation Of Memory Mapping Algorithm To Support Flexible Decoder Architecture",** *IEEE International Conference on Acoustics, Speech and Signal Processing (ICASSP)*, 2013

P. Burgio, A. Marongiu, R. Danilo, P. Coussy, L. Benini, **"Architecture and Programming Model Support for Efficient Heterogeneous Computing on Tightly-Coupled Shared-Memory Clusters",** *IEEE International Conference on Design and Architectures for Signal and Image Processing (DASIP),* 2013

A. Briki, C. Chavet, P. Coussy **"A Memory Mapping Approach for Network and Controller Optimization in Parallel Interleaver Architectures"**, *ACM Great Lakes Symposium on VLSI on VLSI (GLSVLSI)* 2013.

P. Burgio, M. Andrea, L. Benini, C. Chavet, P. Coussy, D. Heller, **"OpenMP-based Synergistic Parallelization and HW Acceleration for On-Chip Shared-Memory Clusters"**. *15th Euromicro Conference on Digital System Design: Architectures, Methods & Tools (DSD)*, 2012.

A. Briki, C. Chavet, P. Coussy, E. Martin, **"A Design Approach Dedicated to Network-Based and Conflict-Free Parallel Interleavers"**, *ACM Great Lakes Symposium on VLSI on VLSI (GLSVLSI)* 2012.

O. Sanchez, S. Reehman, S. Awais, C. Chavet, P. Coussy, M. Jezequel, C. Jego, "**Dedicated approach to explore design space for hardware architecture of turbo decoders"**. *IEEE Workshop on Signal Processing Systems (SIPS)* 2012.

A. Sani, P. Coussy, C. Chavet, E. Martin, **"A Methodology based on Transportation Problem Modeling for Designing Parallel Interleaver Architectures"**, *IEEE International Conference on Acoustics, Speech and Signal Processing (ICASSP)*, 2011.

A. Sani, P. Coussy, C. Chavet, E. Martin, **"An Approach Based on Edge Coloring of Tripartite Graph for Designing Parallel LDPC Interleaver Architecture"**, *IEEE International Symposium on Circuits and Systems (ISCAS)*, 2011.

A. Sani, P. Coussy, C. Chavet, E. Martin, **"Design of Parallel LDPC Interleaver Architecture: A Bipartite Edge Coloring Approach"**, *IEEE International Conference on Electronics, Circuits, and Systems (ICECS)*, 2010.

G. Lhairech-Lebreton, P. Coussy, D. Heller, E. Martin, **"Bitwidth-Aware High-Level Synthesis for Designing Low-Power DSP Applications"**, *IEEE International Conference on Electronics, Circuits, and Systems (ICECS),* 2010.

V. Lefftz, J. Bertrand, H. Cassé, C. Clienti, P. Coussy, L. Maillet-Contoz, P. Mercier, P. Moreau, L. Pierre, E. Vaumorin, **"A Design Flow for Critical Embedded Systems"**, *IEEE Symposium on Industrial Embedded Systems (SIES)*, 2010.

G. Lhairech-Lebreton, P. Coussy, E. Martin, **"Hierarchical and Multiple-Clock Domain High-Level Synthesis for Low-Power Design on FPGA"**, *IEEE International Conference on Field Programmable Logic and Applications* (FPL), 2010.

C. Chavet, P. Coussy, P. Urard, E. Martin, **"Static Address Generation Easing: a Design Methodology for Parallel Interleaver Architectures"**, *IEEE International Conference on Acoustics, Speech and Signal Processing (ICASSP),* 2010.

C. Chavet, P. Coussy, **"A Memory Mapping Approach for Parallel Interleaver Design with Multiples Read and Write Accesses"**, *IEEE International Symposium on Circuits and Systems (ISCAS),* 2010.

P. Coussy, A. Rossi, M. Sevaux, K. Sörensen, and K. Trabelsi, **"VNS for High Level Synthesis"**, *In Proceedings of 8th Metaheuristics International Conference, MIC 2009,* July 2009.

C. Chavet, C. Andriamisaina, P. Coussy, E. Casseau, E. Juin, P. Urard, E. Martin, **"A Design Flow Dedicated to Multi-mode Architectures for DSP Applications"**, *IEEE International Conference on Computer Aided Design, (ICCAD)* 2007.

C. Chavet, P. Coussy, P. Urard, E. Martin, **"Application of a design space exploration**

tool to enhance interleaver generation", *European Signal Processing Conference (EUSIPCO)* 2007.

F. Thabet, P. Coussy, D. Heller, E. Martin, **"Behavioral Description Model BDM for Design Space Exploration: a Case Study of His Algorithm for MC-CDMA System"**, *European Signal Processing Conference (EUSIPCO)* 2007.

C. Chavet, P. Coussy, P. Urard, E. Martin, **"A Methodology for Efficient Space-Time Adapter Design Space Exploration: A Case Study of an Ultra Wide Band Interleaver"**, *IEEE International Symposium on Circuits and Systems (ISCAS)*, 2007.

C. Andriamisaina, P. Coussy, E. Casseau, **"Synthesis of Multimode digital signal processing systems"**, *NASA/ESA Conference on Adaptive Hardware and Systems (AHS)*, 2007.

C. Chavet, P. Coussy, P. Urard, E. Martin, **"A Design Methodology for Space-Time Adapter"**, *ACM Great Lakes Symposium on VLSI on VLSI (GLSVLSI)*, 2007.

F. Thabet, P. Coussy, D. Heller, E. Martin, **"Design Space Exploration of DSP Applications Based on Behavioral Description Models"**, *IEEE Workshop on Signal Processing Systems Design and Implementation (SIPS)*, 2006.

L. Kriaa, S. Adriano, E. Vaumorin, R. Nouacer, F. Blanc, S. Pajaniardja, P. Coussy, E. Martin, D. Heller, F. Thabet et al , **"SystemC'mantic : A high level Modeling and Co-design Framework For Reconfigurable Real Time Systems"**, *Forum on Design Languages (FDL)*, 2005.

P. Coussy, G. Corre, P. Bomel, E. Senn, E. Martin, **"A More Efficient and Flexible DSP Design Flow from MATLAB-SIMULINK"**, *IEEE International Conference on Acoustic, Speech and Signal Processing (ICASSP)*, 2005.

P. Coussy, G. Corre, P. Bomel, E. Senn, E. Martin, **"High-level synthesis under I/O Timing and Memory constraints"**, *IEEE International Symposium on Circuits And Systems (ISCAS)*, 2005.

P. Coussy, D. Gnaëdig, A. Nafkha, A. Baganne, E. Boutillon, E. Martin, **"A Methodoly for IP integration in DSP Soc: a case study of a MAP algorithm for turbo decoder"**, *IEEE International Conference on Acoustics, Speech and Signal Processing (ICASSP)*, 2004.

F. Abbes, E. Casseau, M. Abid, P. Coussy, J.-B. Legoff., **"IP integration methodology for SoC design"**, *International Conference on Microelectronics (ICM)*, 2004.

F. Thabet, J.-B. Legoff, P. Coussy, E. Martin, **"A Methodoly for Timing and Structural Communication Refinement in DSP Systems"**, *International Conference on Microelectronics (ICM)*, 2004.

P. Coussy, A. Baganne, E. Martin, **"Communication and Timing Constraints Analysis for IP Design and Integration"**, *IFIP WG 10.5 Very Large Scale Integration of System-on-Chip Conference (VLSI-SOC)*, 2003.

P. Coussy, A. Baganne, E. Martin, **"Virtual Component IP Re-use in Telecommunication Systems Design: A Case Study of MPEG-2 / JPEG2000 Encoder"**, *IEEE International Conference on Electronics, Circuits, and Systems (ICECS)*, 2002.

P. Coussy, A. Baganne, E. Martin, **"IP Cores Integration in DSP System-On-Chip Designs"**, *European Signal Processing Conference (EUSIPCO)*, 2002.

P. Coussy, A. Baganne, E. Martin, **"Platform-Based Design For Digital Signal Processing Systems: A Case Study of MPEG-2 / JPEG2000 Encoder"**, *IEEE International Conference on Communication Circuits and Systems (ICCCAS)*, 2002.

P. Coussy, A. Baganne, E. Martin, **"A Design Methodology for IP Integration"**, *IEEE International Symposium on Circuits and Systems (ISCAS)*, 2002.

P. Coussy, A. Baganne, E. Martin, **"A Design Methodology for Integrating IP into SOC Systems"**, *IEEE International Custom Integrated Circuits Conference (CICC)*, 2002.

G. Savaton, P. Coussy, E. Casseau, E. Martin, **"A Methodology for Behavioral Virtual Component Specification Targeting SoC Design with High-Level Synthesis Tools"**, *In Proc. of the Forum on Design Languages (FDL)*, 2001.

S. Pillement, O. Sentieys, D. Chillet, E. Casseau, P. Coussy, E.Martin, G. Savaton, S. Roux, **"Design and synthesis of behavioral level virtual components"**, *IFIP WG 10.5 Very Large Scale Integration of System-on-Chip Conference (VLSI-SOC)*, 2001.

International Conferences (invited)

P. Coussy "**High-Level Synthesis, Architecture and Programming Model Support for Efficient Heterogeneous Computing on Tightly-Coupled Shared-Memory Clusters**",

International Workshop on "Electronic System-Level Design towards Heterogeneous Computing", IEEE Design Automation and Test in Europe DATE, March 2014

P. Coussy, panellist in "**Applying High-Level Synthesis (HLS) in an SoC Flow**", *EE Times Virtual Event: System-on-Chip 2011,* May 12th, 2011.

P. Coussy **"An Introduction to High-Level Synthesis"**, *Embedded tutorial "An Introduction to the SystemC Synthesis Subset Standard", IEEE International Conference on Hardware-Software Codesign and System Synthesis (CODES+ISSS)*, Scottsdale, USA, October 2010.

P. Coussy, **"High-Level Synthesis of dedicated of dedicated coprocessors"**, *Tutorial on ESL Design and Virtual Prototyping of MPSOCs, IEEE Design Automation Conference DAC* Anaheim, USA, June 13th, 2009.

P. Coussy, **"Multi-Mode Architecture Design with High-Level Synthesis"**, *Workshop on High-level synthesis, IEEE Design Automation and Test in Europe DATE*, March 2008.

P. Coussy, **"GAUT: A High-Level Synthesis Tool"**, *Workshop on High-level synthesis, ECSI Institute & UBS Workshop*, September 18th, 2006.

French speaking Conferences

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