

Contact: Vincent Lefftz

vincent.lefftz@astrium.eads.net, Astrium Satellites Toulouse

The evolution of the technology and the application needs leads to design more and more complex embedded systems both at hardware level and software level.

Mastering this complexity, in order to improve the time cycle and the costs of the design and the validation/certification of the critical embedded systems, is a key point to ensure the success of future industrial projects.

Issues

Indeed, the **mastering of a "seamless" design flow** built upon a **set of integrated engineering tools**, allowing to validate/qualify/certify any critical embedded systems based on SoC (System On Chip) is needed for aeronautic, space, energy, automotive and health applications.

Our ambitions

- Combine the partners effort to propose some methodological and process solutions for the full design flow of critical embedded systems, by using the cross-competencies of the industrial and academic partners
- Define a "seamless" development flow, integrating the equipment qualification/certification, from the system level to the Integrated Circuits (IC) and associated SW
- Master the "system dimension" (SW + HW) into the SoC integration issues

- Master the complexity, the time cycle reduction, the design optimization of SoC-based systems
- Evaluate the HW simulation models (from the design flow) usage for the integration and the validation of the critical embedded SW
- Propose a prototype of an Integrated Development Environment based on open standards of the market, implementing the SoCKET process and adaptable with other tools and for other application domains



« Seamless » flow

- Classical process System Specifications Fystem Specifications System Specifications Fystem Specifications Fys
- High level synthesis
- Heterogeneous simulation techniques (SystemC/TLM)
- IPs encapsulation & interoperability (IP-XACT/OCP-IP)
- Formal verification by model-checking
- Semi-formal methods by automatic generation of monitors
- Mutation analysis techniques
- Test cases automatic generation
- Solution based upon market open standards (SystemC/SPIRIT)

Key figures

Duration: 36 months (06/2008 - 06/2011)

Budget: 10.7 M€