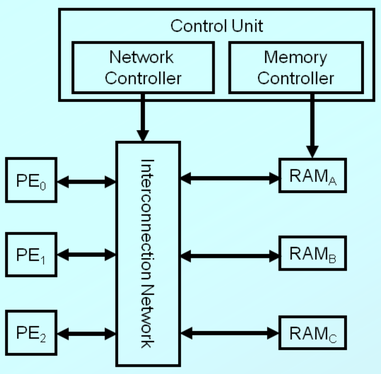
Embedding polynomial time Memory Mapping and routing Algorithms on-chip to design configurable Decoder Architectures

Saeed Ur -REHMAN, Awais SANI, Cyrille CHAVET, Philippe COUSSY
Lab-STICC, Université de Bretagne Sud, CNRS UMR 6285. {FirstName.LastName@univ-ubs.fr}

Problem Formulation



	t_0	t_1	t_2	t_3	t_4	t_5
PE_0	1	1	8	5	5	7
PE_1	2	2	5	6	2	1
PE_2	3	6	4	7	6	2
PE_3	4	4	1	3	3	3

Time (t_y cycles)

Parallel decoder architectures are composed of P processing elements $PE_x$and P memory banks RAM_y that process and store L data.

Memory accesses are represented as a matrix. Lines represent the set of data used by each PE. Columns represent processing time instances.

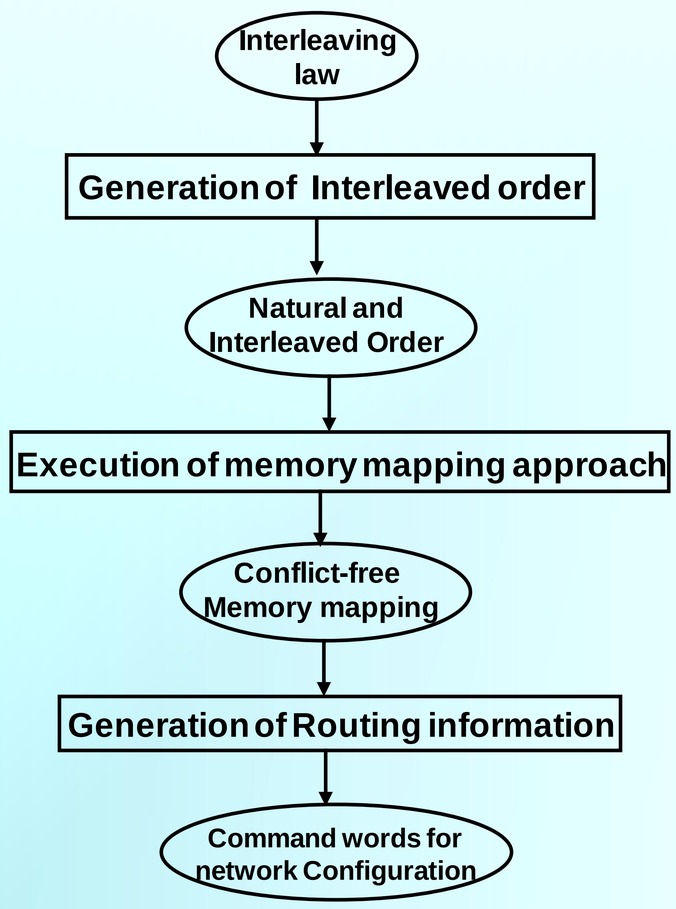
The problem is to find a memory mapping avoiding memory access conflicts

Related Works

	Any Standard	Architecture complexity	Algorithm complexity
Gnaedig *et al.*	NO	Low	High
Tarable *et al.*	YES	High	High
Wehn *et al.*	YES	High	Medium
Muller *et al.*	YES	High	Medium
Briki *et al.*	YES	High	Medium
Sani *et al.*	YES	High	Low
Our approach	**YES**	**Low / Medium**	**Low**

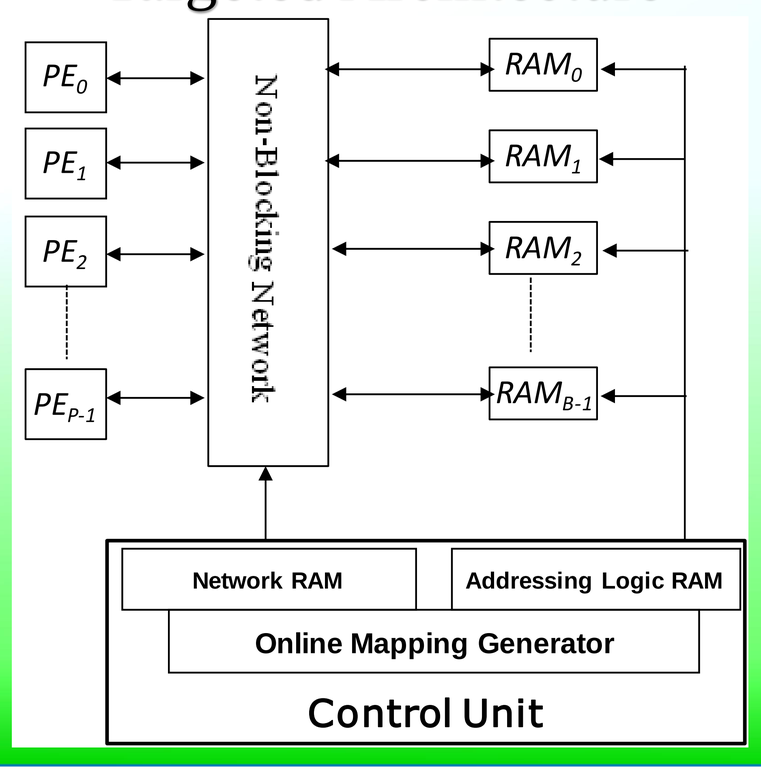
Proposed Design Flow

In order to be able to deal with more and more complex and multi-standard architectures, with an affordable cost, our goal is to build a configurable interleaver architecture.



The idea is to replace interleavers by an embedded conflict free mapping and routing algorithm.
Significant reduction in time and memory cost can be obtained by embedding polynomial time memory mapping algorithm on-chip compared to state of the art approaches.

Targeted Architecture



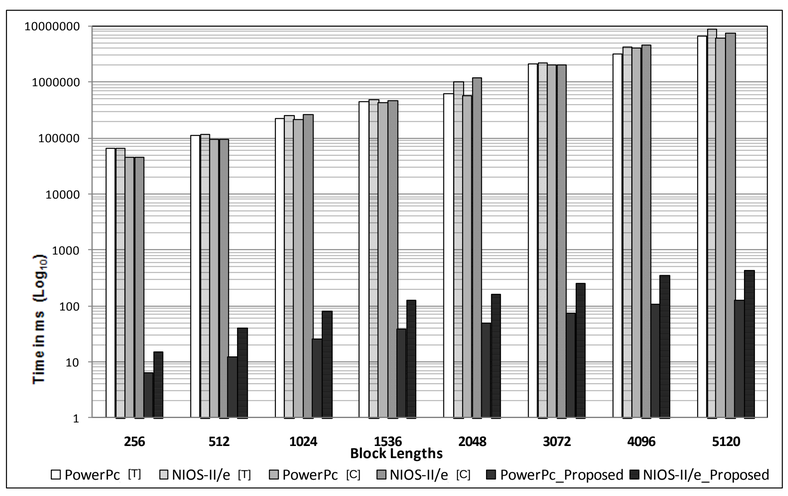
Test cases

Different experiments have been performed using different embedded processors (PowerPC and NIOS-II) to measure the runtime performances:
- PowerPC is a hard processor embedded in Xilinx Virtex-5 ML507
- NIOS-II is an embeded soft core in Altera FPGAs.

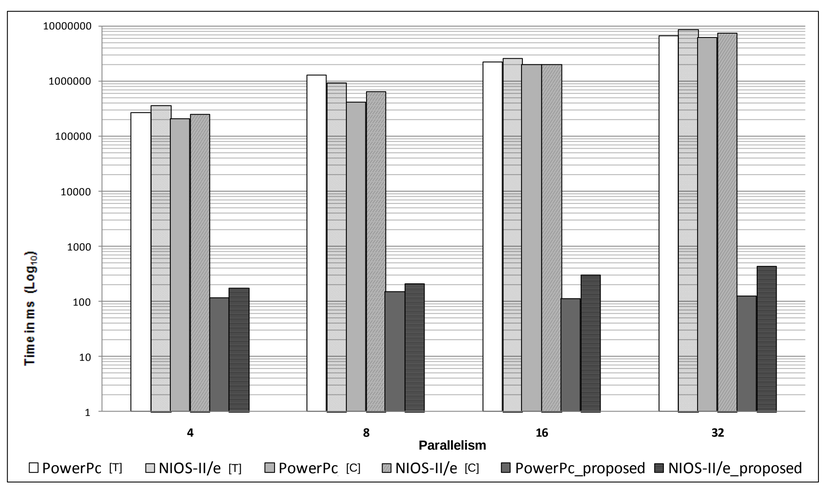
Test case: HSPA interleaver used in 3GPP-WCDMA

Analysis of rune time performances for several block length and parallelism, and comparison for architectural costs compared to our on-chip memory mapping approach.

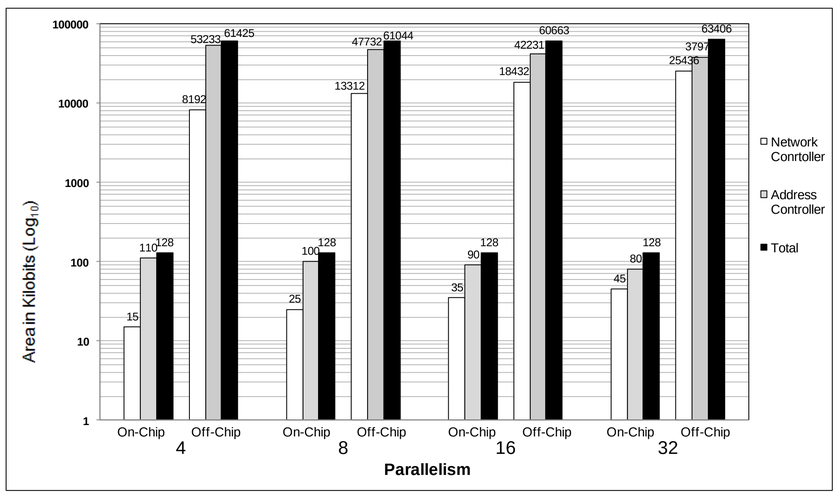
Results



Normalized Run time Values (Block 256, Parallelism 32)



Normalized Run time Values (Block 5120, several Parallelism)



Area Comparison for on-chip and off-chip mapping

[T]: Tarable et al, IEEE Trans.Inf.Theory 2004

[C]: Chavet et al, ICASSP 2010

Conclusion

We proposed to embed polynomial time memory mapping approach and routing algorithm on-chip to solve memory conflict problem in parallel hardware decoders based on Benes network. Experiments shown that the proposed approach allows to greatly improve timing performances and to reduce memory footprint. Future work is to further improve the execution time by using ASIP or hardware accelerators to target real time flexible decoder architectures.

« We can't solve problems by using the same kind of thinking we used when we created them » - Albert Einstein