Speaker:
Greg Stitt

Title:
FPGA Virtualization Strategies for Mainstream High-level Synthesis

Abstract:
Although the advantages of FPGAs compared to GPUs and multi-cores have been widely shown for various domains, mainstream application designers have resisted FPGAs due to significant application design complexity. Although high-level synthesis (HLS) reduces complexity, several critical limitations have prevented mainstream usage. One increasingly significant limitation is lengthy compilation times ranging from hours to days, which reduces productivity and prevents mainstream design methodologies. A second limitation is limited HLS support for different devices and boards. As a result, HLS-generated applications often leave many device- and board-level resources unused or underutilized, which can force designers to resort to more complex register-transfer-level design.

To address these challenges, this talk will discuss virtualization strategies that reduce the semantic gap between high-level applications and fine-grained FPGAs. Whereas physical FPGAs contain hundreds of thousands of fine-grained resources to maximize flexibility, virtual FPGA systems, which are implemented atop such physical FPGAs, can be specialized to the needs of different application domains to hide physical device and board complexity. As a result, virtualization enables rapid FPGA compilation that can complete in seconds as opposed to hours. Virtualization also enables application portability across physical FPGAs, similar to how virtual machines achieve portable software code, in addition to enabling any HLS tool to effectively target any FPGA system. By combining virtualization with high-level synthesis from standardized parallel languages (e.g., OpenCL), the presented strategies enable mainstream FPGA usage by enabling design flows used by other mainstream computing devices.