Reliable ASIC (RELIASIC)

Towards next generations of architecture and design flow to perform signal processing applications with unreliable components: case study on GPS architecture.

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Contents

Chapter 1

Context, position and objectives of the proposal

1.1 Problem addressed and motivation

One of the most critical challenges of the ITRS overall design technology (2010) is fault-tolerant computation. The increase in integration density and the requirement of low-energy consumption can only be sustained through low-powered components, with the drawback of a looser robustness against transient errors. In the near future, electronic gates to process information will be inherently unreliable.

In this project, we want to address this problem with a bottom-up approach, starting from an existing application (a GPS receiver) and adding some redundant mechanisms to allow the GPS receiver to be tolerant to transient errors due to low voltage supply.

Our objective is to produce an ASIC with two versions of the application: a standard GPS receiver and a hardened GPS receiver (a simple L1 band GPS receiver). Our ambition is to decrease by a **factor of 4** the energy of the hardened GPS receiver thanks to a very low power supply voltage while keeping an acceptable degradation of the quality of service provided by the device (i.e. Mean Time of First Fix (few tens of seconds)[1] and the variance of the error position estimation (few tens of meters).

To interpret this in terms of world energy savings, we assume on the order of 10 billion GPS receiver units in the world in the near future (a conservative hypothesis), each working 1% of the time. Each mW saved with fault tolerant design will give a global saving of 10^{-6} (1 mW express in KW) $\times 10^{10}$ (number of GPS) $\times 10^{-2}$ (rate of utilisation) $\times 24 \times 356$ (number of hours in a year) $= 0.88 \times 10^6$ KW.h per year in the world[2]. Note also that GPS are mainly used in application that implies mobility. Mobile devices don't have direct access to powerline energy and should use batteries and/or produce directly its own electrical energy (energy harvesting devices). In both cases, the cost and the enviromental impact to provide energy is high.

During this project, we will develop knowledge at several levels: the effect of low voltage at transistor level, application of robust non-conventional arithmetic, the downstream impact of gate level errors on arithmetic and functional operation, refinement of high level specification (reliability and quality of service) to low level arithmetic and functional requirements. Measurement of the ASIC product will allow us to test the proposed methods on a real design case and provide very useful feedback.

[1] The mean time between a cold start, with no a priori information on the actual position and the first position given by the GPS receiver

[2] For comparison, the average energy consumption of a familly in France is 6.7×10^3 KW.h per year

The RELIASIC project will trigger a scientific community in the area of fault-tolerant computation for very low power processing with the focus "Energy and resource efficiency in ICT" of the Labex CominLab. As a longer research perspective, the consortium wants to capitalize on this project by extending the knowledge obtained with the RELIASIC bottom-up approach to define new computation methods, new design methodology and tools for fault-tolerant computation.

1.2 State of the art

Nanoscale systems have become more and more sensitive to Process, Voltage and Temperature variations (the so called PVT variation) [1]. With such PVT variations, requiring exact computation in a circuit implies undesirably high supply voltage and reduced yield production. It is potentially far more efficient to embed in the circuit error resiliency capacities to cope with low voltage, and to obtain high yield circuits compliant with the PVT variations.

Research on computation on unreliable computing is as old as electronics. In fact, Von Neuman has proposed a theoretical solution to the problem in 1956 [2]. The idea is to use a set of N wires to represent a given information. Logic functions are also duplicated N-times. Then a restoration process is applied to reduce the error probability of the output functions. The restoration process triplicates each function output to generate $3N$ wires, which are interleaved in a random way. A new N-wire signal is then reconstructed using N noisy 3-input majority gates. If the error probability of the function and the 3-majority gate is low enough (NAND gate with a probability of error around 0.01), perfect computation can be performed when N goes towards infinity. The problem of this method is that the hardware efficiency (the average amount of computation per time unit and area unit) goes towards zero, which is not acceptable in practice.

Over almost 60 years, the problem of computation on unreliable architecture has been studied, mostly for applications working in high radiation environment (e.g. space and nuclear applications) and/or requiring very high level of reliability (e.g. aircraft control). Recently, the area of fault-tolerant computation has spread in general purpose applications. In "Error-resilient systems via statistical signal processing," [3], R. Abdallaf and N. Shanbhag present a very interesting survey of modern fault tolerant techniques. They claim potential savings of 3 to 6$\times$ in energy thanks to an efficient integration of redundancy in few critical parts of a digital design.

1.3 GPS receivers at a glance

A GPS is a well spread technology that allow to dertermine both the local physical position and the absolute time of a receiver. The 4 parameters of the position (3 for space, 1 for time) are determined thanks to a precise distance measurement with at least four GPS satellites. Each GPS satellite transmits in BPSK its own speudo-random sequence of length 1023 (1023 chips) every millisecondes. For each satellite that are visible in the sky, the receiver demodulates this signal and thus, is able to determine precisely the time of arrival of a given satellite. From the time of arrival of different satellites, the receiver is able to solves geometrical equations to determine its own position. Of course, once detected, a satellite signal needs to be tracked in order to follow the evolution of the distance and to demodulate the 50 bit/s associated message.

RELIASIC is focused on hardning techniques. To save time in the projet, we will use an existing design developped in the Institut Superieur de l'Aéronotique et de l'Espace (ISAE) in a frame of the funded project. The acquisition part of the ISAE' GPS architecture is based on Akopian architecture [4], with the parameters described in [5].

Figure 1.1 shows the acquisition part. This module tries to synchronise in a blind way (i.e. brute force approach) in time (with a precision of half chip, i.e. 2046 possible positions) and frequency (with a precision of 50 Hz in a dynamic range of ± 4 KHz due to Doppler shift, i.e. 160 different positions in frequency) to each satellite of the GPS constellation.

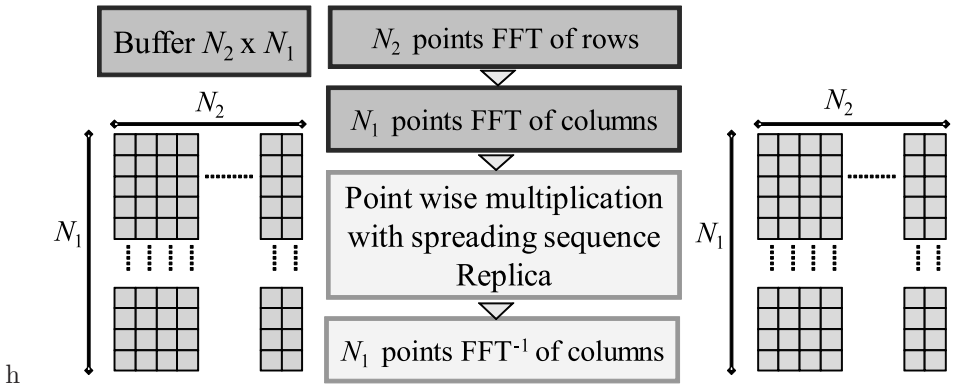

Figure 1.1: Architecture of acquisition module

As shown in figure 1.1, this architecture is based on FFT. The first 2-D FFT (heavy grey, in the upper part of the figure), is shared for the detection of all satellites in a given doppler range while the IFFT (light grey, in the botom part) is dedicated to the detection of a given satellite and is repeated 32 times (maximum number of satellites in the GPS constellation). Figure 1.2 show a typical output of acquisition processing for a given satellite. The position of the peak of energy gives the time and frequency information about the satellite.

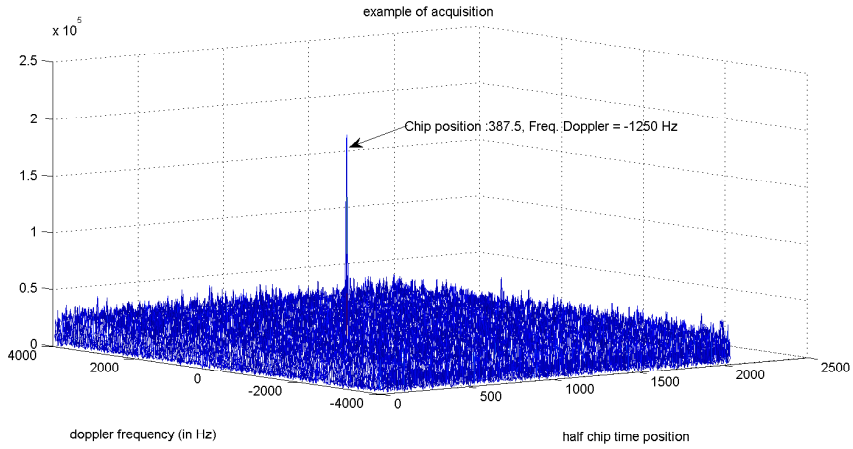

Figure 1.2: Example of acquisition output

Clearly, a significant error in the first 2D-FFT will prevent detection of any satellite for this slot of time and range of Doppler frequency while an error in the second one will only prevent the detection of the satellite, or give a wrong acquisition position. Those two types of errors don't have a catastrophic effect on the GPS receiver. In fact, each satellite is checked periodically, each miss detection (or wrong detection) only delay the real acquisition of the satellite. This degradation is admissible (at a given level) in our low power design philosophy.

Figure 1.3 shows the tracking architecture, i.e., a feedback loop that tracks the variation of distance and that also perform demodulation of the signal (each satellite sends its own ephemerid, clock correction and the GPS constellation almanac at 50 bit/s). The first NCO (Numerically Controled Oscillator) supresses the rotation of sampled signal due to the Doppler frequency shift. The second NCO is used to despread the signal (PN the pseudo random spreading sequence associated to the GPS satellite). Three versions of PN sequence are generated: one with a little advance (Early), one with a little time delay (Late) and the last one in time (In Phase, or Prompt). The output of the three corellators are first integrated on 1 ms (time of repetition of the spreading

sequence). The variation of energy on Early, Late and Prompt ouputs allow to track the time drift. Then the next integration of 20 ms allows to decode a modulated bit with a rate of 50 bit/s.

An error in the tracking module can lead to an error of position but, fortunatly, it essentially does repetitive computations, since the evolution of time and Doppler frequency drift is slow. In other words, there is a lot of time redundancy in the tracking processing that can be efficiently exploited to support transient errors.

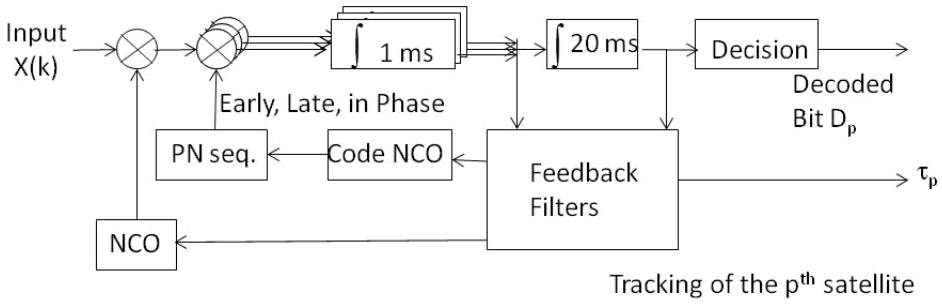

Figure 1.3: Tracking architecture

The last part of the GPS is a soft program that gives the position based on the measure delay values and ephemerid information. This task is complex but performed only every second: a software implementation is thus natural. This task will be considered out of the scope of the project (signal processing on unreliable hardware). An error free external software connected to the chip will compute the position.

1.4 Expected contributions

There are five expected contributions on the project:

- A first contribution of the project is to develop error models based on low level simulation of CMOS devices with very low voltage.
- A second contribution of the project is to develop unconventional methods to perform signal processing computation on unreliable hardware. Those unconventional methods will include stochastic computation, hybrid dual module systems, and residue and redundant number systems.
- A third contribution of the project is is to evaluate the impact of errors on hardware units used for signal processing. We will focus on arithmetic operators. Two approaches will be investigated: a theoretical analysis based on operator behavior models and an experimental approach based on emulation.
- A fourth contribution of the project is to refine high level specifications to include low level requirements that guaranty an overall behavior. The high level specification can be: 1) an acceptable level of degradation of performance, 2) a mean time between failures (no more useful output generated).
- The fifth and last contribution of the project is to build a demonstration case to validate the fault-tolerant techniques proposed in the project. Two versions of the GPS receiver will be implemented on an ASIC in a 28 nm technology. Extended measurement will allow characterizing the behavior of both receivers in terms of power dissipation and quality of service when the powers supply voltage decrease. The ASIC will probably be pad limited, which will give us the opportunity to implement a set of standalone key components of the project and to test them individually.

These five contributions will be addressed by five workpakage activities. Figure 1.4 shows in a synthetic way the link between those 5 WP.

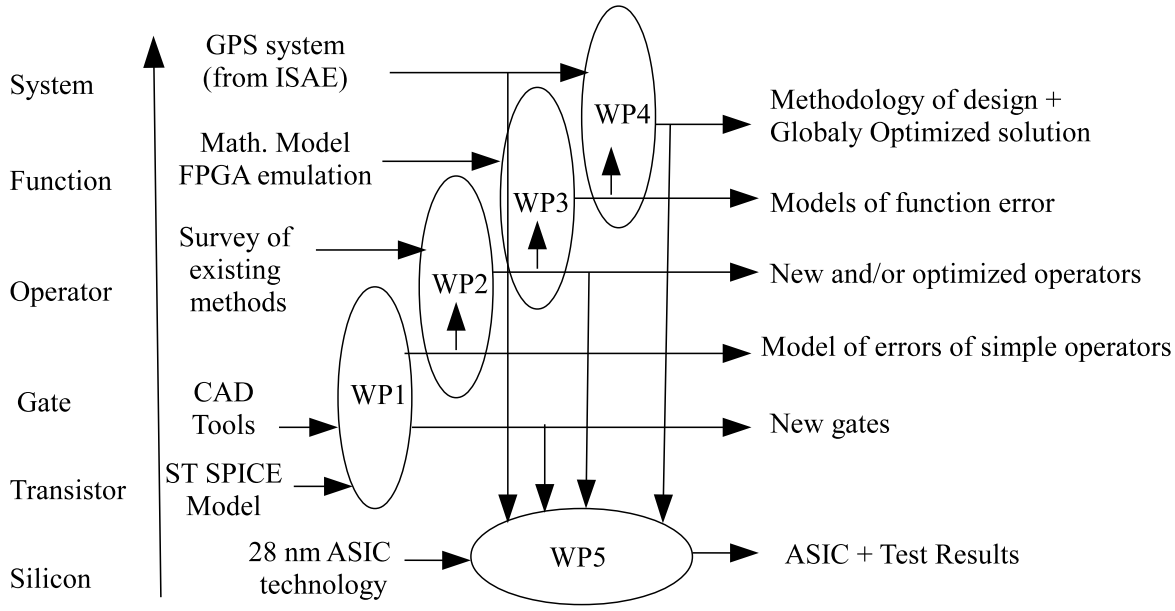

Figure 1.4: Structure of the project

1.5 Relevance of RELIASIC to the objectives of CominLabs

One of the main objectives of the RELIASIC project is to be able to free the constraint of "error free" design by construction and condition of utilization with "error acceptable" design by smart architecture and design process. A straightforward application of the knowledge generated by the project will be to decrease the circuit's supply voltage to obtain a significant decrease of power dissipation, while maintaining a guaranteed level of quality of service. This objective falls right in the scope of the focus 3 of CominLab, i.e. "Energy and resource efficiency."

More generally, the objective of CominLab is to structure the scientific community of Bretagne and Pays de Loire in the area of Information and Communication Technologies (ICT) and lead to worldwide recognition in new scientific areas. We believe that the RELIASIC project falls right in this objective: we propose to join complementary expertise spread between Brest, Lannion, Lorient, Nantes and Rennes to address this challenge.

1.6 Consortium

The consortium will be leaded by E. Boutillon, professor at the University of Bretagne Sud.

The consortium is based on 3 laboratories, all associated to the CNRS, and a professor from Utah State University:

- Lab-STICC (Laboratoire des Science et Technologie de l'Information, Communication et Connaissance, UMR 6285), CACS (Communications, Architectures, Circuits and Systems) department.
- IETR (Institut d'Electronique et de Telecommunications de Rennes, UMR 6164) team SCN (located both in Nantes and Rennes).

- IRISA (Institut de recherche en informatique et systemes aleatoires, UMR 6074), CAIRN research group.

Those 3 laboratories have complementary expertise for the project. All of them have recognition in signal processing and hardware design, with some specializations.

This project will also be done in association with Professor Chris Winstead, from Utah State University. Chris Winstead is at the moment in Lab-STICC for a sabbatical year (June 2013-June 2014), funded with a Fulbright Grant. His research project during his sabbatical concerns ultra low power processing. He will simultaneously send a proposal to NSF (in January 2014) on ultra low power design, with a connection to RELIASIC to allow the exchange of PhD students from both sides of the Atlantic. This will be an opportunity to continue the collaboration initiated during the sabbatical stay in Lab-STICC.

See section 3 for more details on the laboratories.

1.7 Resources

The resources for the main project are summarized in the next table:

Ressource	Lab-STICC			IETR		IRISA	total
	TB	UBO	UBS	INSA	Nantes	UR1	
PhD 1	100						100
PhD 2			100				100
PhD 3						100	100
PhD 4					100		100
Eng. WP5	60						60
7 trainees	2.5	2.5	2.5	5	2.5	2.5	17.5
ASIC run	40						40
Expenditures	15	2.5	15	4	15	15	66.5
Total	217.5	5	117.5	9	117.5	117.5	584

Table 1.1: Resources for the project (in K€)

1.7.1 Project scheduling

The duration of the project is 4 years. The first 3 years will be dedicated to the research in WP 1 to 4. WP5 will start at T + 30 in order to obtain a layout at T+36. Then, after 3 months for the fabrication of the ASIC, the remaining 9 months of the project will be dedicated to experimental measurement on the ASIC.

During the project, 5 general meeting are scheduled, respectively at T_0, $T_0 + 12$, $T_0 + 24$, $T_0 + 36$ and the final meeting at T0+48. The members of CominLabs will be informed of the date of the meeting, and, of course, cordially invited to participate. During the kick-off meeting (T_0), a trainning session on GPS algorithm and architecture will be organized. All WP leader will also present a updated start of the art. The generic agenda of the following meeting includes 1) PhD students work-status; 2) WP work-status; 3) publication/diffusion strategy; 4) action plan for the next year; 5) public or industrial funding opportuniies to extend the project. The final meeting ($T_0 + 48$) will be dedicated to the final presentation of the project and open to our scientific communauty.

In complement with those formally annual meeting, we will have a monthly phone meeting in order to follow the advance of the project. Of course, many intra and inter WP meetings will be

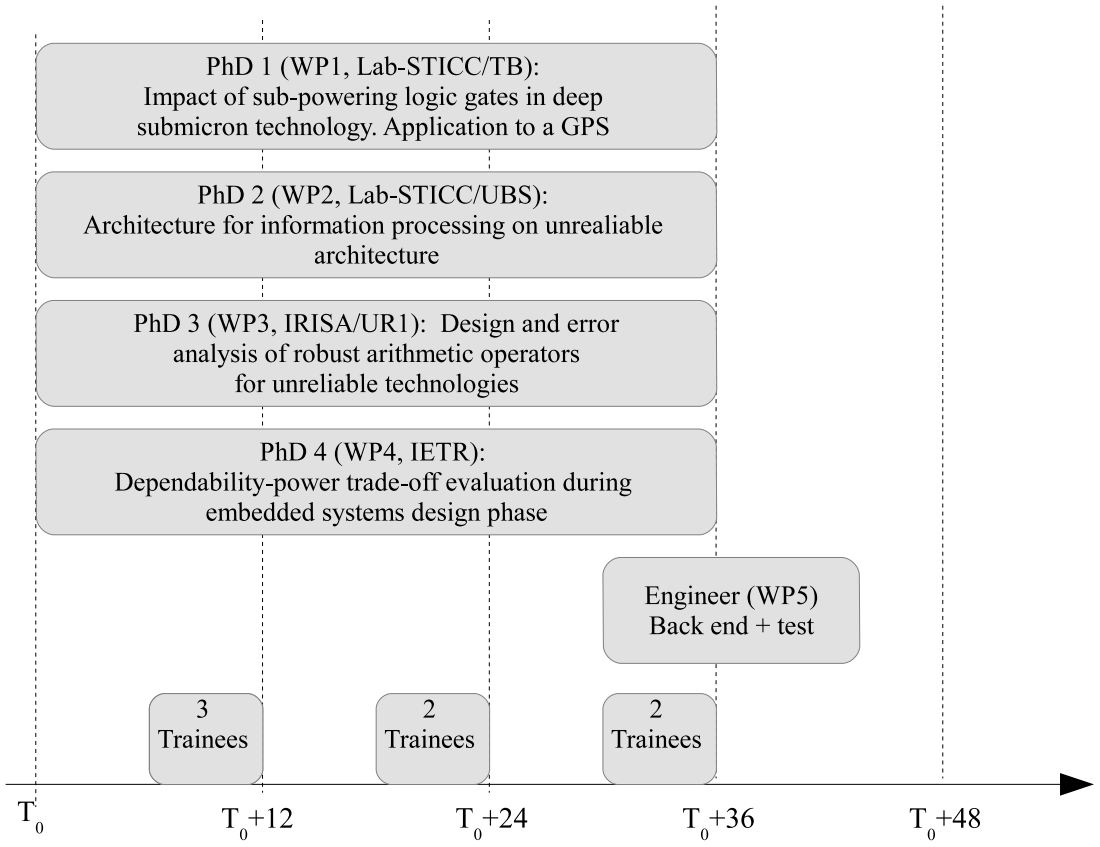

Figure 1.5: Human ressources scheduling

organized during the project. These meetings will be decided on the fly according to the necessity of the project.

In order to follow the evolution of the project, 4 milestones are defined:// Milestone 1 (T_0+12): reference model of the basic GPS architecture as well as performance estimation versus power dissipation as a function of power supply tension.
Milestone 2 ($T_0 + 24$): selection of the set of techniques used for the robustified version of the GPS.
Milestone 3 ($T_0 + 36$): tape out of the ASIC.
Milestone 4 ($T_0 + 48$): feedback from the measurement of the ASIC.

Finally, figure 1.5 shows the allocation of the human resources asked for the project:

The previsional list of trainee projects is:

- Trainee 1 (WP5, Lab-STICC/UBS): Implementation of the tracking module for the reference GPS.
- Trainee 2 (WP3, IRISA/UR1): Impact of the representation of numbers on the fault detection/tolerance capabilities of sequences of arithmetic computations.
- Trainee 3 (WP1, Lab-STICC/TB): impact of noise sources in CMOS elementary gates in subtreshold operations.
- Trainee 4 (WP4, Lab-STICC/UBO): Models to analyse trade-off between reliability and power dissipation in a GPS application.

- Trainee 5 (WP4, IETR/SCN, INSA-Rennes): Impact of dependability on embedded systems performances.
- Trainee 6 (WP4, IETR/SCN, INSA-Rennes): Energy power consumption model of protected applications.
- Trainee 7 (WP4, IETR/SCN, Polytech Nantes): High-level model of unreliable silicon.

Chapter 2

Scientific program

The project is divided in 5 work packages, as shown in figure 2.1

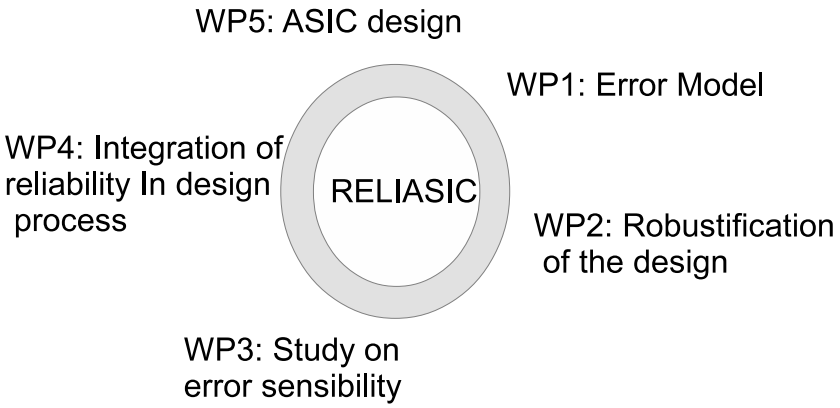

Figure 2.1: Global WP organization

For each work-package, we will describe the scope of the WP, the expected results and the link with others' work-packages. We will also indicate the resources (researchers and funding) allocated to each WP.

2.1 WP1: Error model

WP1 is lead by Fabrice Seguin, from Lab-STICC/CACS (Télécom Bretagne).

2.1.1 Task description

In this work package we characterize the impact of lowering the power on logic gates in a 28 nm CMOS technology.

Task 1: In deep submicron technologies, several noise sources like random telegraph noise, thermal noise, or shot noise, must be particularly investigated and modelized. These sources should be considered in order to evaluate their impact especially when the transistors operate in sub-threshold region that is actually the case when sub-powering. Several studies in this topic [6–8]

shows for instance an instability in the threshold voltage. But those effects are not really well taken into account in the simulation software tools. A goal in this task is to improve the accuracy of the electrical simulation by including those noise sources in the tools. We will next focus on basic gates, constituting specific operators, that are used in GPS function. After a state of the art on the behavior of the elementary gates in nanoscale technologies, each basic cell will be electrically characterized in order to obtain the probability of error as a function of the size of transistors and the supply voltage. The error models will study the influence of deliberate sub-powering of integrated circuits. How sub-powering exacerbates aforementioned errors and generates new errors. Due to lower supply voltages, MOS transistors will often operate in sub-threshold region in forthcoming technologies. This will induce an alteration in basic logic gates behavior. Monte Carlo analysis will also permit to investigate the impact of mismatches between components. And finally PVT simulations will be performed to take into account worst cases for instance. It is important to note that transistor level simulations will be performed in this work package. All simulations will be performed using Spectre models provided by ST Microelectronics for the 28 nm CMOS technology. As a result of the characterization performed in this task, we will develop a behavioral model described in C language, for each digital cell required.

Task2: Based on these results, higher level simulations will be performed in order to obtain models and information about how errors appear and propagate in macro-cells. Those macro cells are critical functions of the GPS and will be defined manually (not generated from synthesis). As a result of the characterization performed in this task, we will develop a behavioral model described in C language, for each macro cell required. These models will include the voltage supply and the transistors sizes as variables. If necessary modified macro standard cells (i.e. hardened circuits) could also be created to facilitate the design of the entire chip in WP5

2.1.2 Interaction with others work packages

This task will result in a document describing in details the origin of each fault, its influence on the integrated circuits functioning and its model. The models will be provided in C language. Those models will be proposed as inputs to WP2, WP4 and WP5.

2.1.3 Partners skills

The researchers involved in this work package have experience in IC design and test. They made a dozen full custom integrated for applications ranging from radio frequencies to channel decoding circuit. They also have experience in system performance degradations due to device and component parasitic elements [9] and logic cell hardening [10].

2.1.4 WP organization and resources

Lab-STICC:

- Fabrice Seguin, Assistant Prof. TB, Cyril Lahuec, Assistant Prof. TB.
- Chris Winstead, Prof. Utah State University.
- 1 PhD student
- 1 Master students (6 months)

2.2 WP2: Robustification of the design

WP2 is lead by Emmanuel Boutillon, from Lab-STICC/CACS (UBS).

2.2.1 Task description

The objective of this task is to demonstrate non-conventional methods at the architecture level to protect vital signal processing functions of a GPS receiver against internal errors. As briefly mentioned in section I, the two tasks of the GPS receivers are acquisition (see figure 1.1) and tracking (see figure 1.3).

In terms of information processing, acquisition module requires:
- state machine (very high reliability),
- input buffer processing (low reliability, since an error in a data will be spread by the FFT),
- FFT processing (medium reliability)
- buffer for the output of the FFT (medium reliability)
- point wise multiplication (low reliability),
- IFFT processing (low reliability)
- maximum energy detection (medium reliability).

The tracking module requires: - state machine (high reliability),
- Numerically Control Operator (NCO) and PN sequence generator (very high reliability),
- Multiplication (low reliability)
- Integrators (medium reliability)
- Feedback loop (high reliability).

Error in the acquisition module will imply miss-detection of a satellite or wrong detection (detection with erroneous time and frequency parameters). In both cases, it implies a degradation of the GPS output (longer time of first fix, fewer satellites used to estimate the position at a given instant) but it could be tolerated up to a specified level. The situation on the tracking module is more complex. Once a satellite detected by the acquisition module, its time acquisition and frequency Doppler estimation is very rough. The tracking module will use a first configuration (with wideband feedback loop) to have a robust and rapid convergence towards a precise enough parameters estimation to start the fine estimation (narrow band feedback loop). In this transitory phase, error reliability should be high. Once locked, the acquisition module starts to do redundant operations ever and ever, tracking only slow variations of time delay and frequency Doppler shift. This time redundancy can be used at a high level to tolerate a rather high rate of internal errors.

To summarize, the GPS application offers us a very interesting set of different signal processing problems, with different requirements of reliability. The goal of WP2 is to study, adapt and create fault detection and/or tolerance techniques for each of the modules identified above. In the following, we present already identified method of the state of the art that will be investigated in this WP.

general problem

The three tasks involved in information processing are:

- transmission of information in time (register, memory)
- transmission of information in space (communication)
- processing of information ($Y = F(X)$)

The first two tasks imply an identity function. If the transmission is noisy, it is possible to combat the noise with the addition of an error control code, since the "processing" is just the identity function, the structure of the code is maintained. At the receiver side, the decoder can correct the transmission errors. Recently, some authors studied the effect of transient error inside the decoder itself. Several results showed that it is possible to construct decoders resilient to internal transient errors [11], [12]. There are several ongoing projects in this area (i-RISC FP7/FET-OPEN (2013-2016), ANR International DIAMOND (2014-2017)).

Reliable processing of information on unreliable hardware is much more challenging. Protection of processing is far more complex, since, in the general case, the structure of a code is not maintain

through a computation F. In others word, if C is the coded version of an input X, $F(X)$ the desired result, there is no simple function F' that gives $F'(C)$ with a linear code structure. The only exception is when the coding process is repetition, which leads to the well known Triple Modular Redundancy (TMR) method for example. Unfortunately, repetition codes are known to be inefficient from an information theory point of view.

Error detection technique

Error detecting technique to detect and error and redo the computation when required (similar to a retransmission in a communication system). For example, the computation of modulo residues in parallel to the main computation for advanced arithmetic operators. The DSP blocks developed in the ARDyT ANR project by IRISA-Cairn team will be used.

At a higher level, properties of an operator can be used to check if the output values are consistent with the input values. For example, the energy between the input vector and the output vector of an FFT operator should be equal. Many errors can be detected using this type of high level method.

Forward error correction techniques

Study of redundant signed digit number systems with specific low-level digit encodings. Redundant arithmetic is widely used in arithmetic operators to allow some errors produced at one iteration which can be corrected during the next iteration (e.g. SRT hardware division unit generator).

Forward error mitigation techniques

The Algorithmic-Noise Tolerance method [13] consists in performing two parallel versions of the processing, the first one with full precision (architecture M_{exact}), the second one with reduced precision (M_{appr}) but higher reliability due to its lower complexity and its design. When the outputs of M_{exact} and M_{appr} are compatible, then it is assumed that no significant errors have occurred and the result of M_{exact} is selected. On the contrary, if the two outputs differ significantly, it means that at least one error occurred. In this case, the output of $M_{appr.}$ is selected since it is by construction more reliable than M_{exact}. An approximation of the correct result is thus output, instead of a faulty one. This method will be studied in particular in the context of the acquisition part.

Stochastic computation techniques

Stochastic computing (SC) performs computations in probabilistic domain by representing binary numbers as random bit streams. A number P between 0 and 1 can thus be represented by a random binary stream of bit with $Prob(b = 1) = P$. As shown in [14], arithmetic operation can be performed with this representation: a simple AND gate with two stochastic input stream P_0 and P_1 will output a stochastic stream $P = P_0 \times P_1$. A simple multiplexer gate with random selection of the input will give and output of $(P_0 + P_1)/2$. This representation is by construction robust to error. Very recently digital filters using stochastic computing have been published [15], [16] with interesting results. The main drawback of stochastic computation is the cost of generation of the random binary streams. We have some experience in this domain (see section 2.2.4) and we expect to develop innovative solutions, especially for the tracking problem.

Conclusion

The problem addressed in WP2 is very exciting and we expect to have several significant contributions, first by the adaptation of the state of the art to solve our particular problem, second, by exploring new unconventional architecture.

2.2.2 Interaction with others work packages

The robust arithmetic circuits proposed in this WP will be evaluated using the two types of methods proposed in WP3 (FPGA emulation and analytical models when possible). Based on

WP4 optimization process, the selected robust arithmetic circuits will be developped in VHDL and used in WP5 to derive the tape-out for the ASIC.

2.2.3 WP organization and resources

IRISA:

- Emmanuel Casseau, Prof. UR1, Arnaud Tisserand, CR CNRS
- 1 PhD student (1/2 time)

Lab-STICC:

- Emmanuel Boutillon, Prof. UBS, Jean-Philippe Diguet, DR, CNRS
- Chris Winstead, Prof. Utah State University.
- 1 PhD student
- 1 Master students (6 months)

2.2.4 Partner skills and background

The IRISA-Cairn team has a strong background in the domain of arithmetic operator study and design including both conventional number systems and advanced representations of numbers [17], [18], [19], [20], [21], [22]. In the reliable architecture field, we proposed computation units with built-in dedicated fault detection resources based on modular arithmetic (residue codes) [BCT13]. We have also designed arithmetic operators based on the residue number system (RNS) for cryptographic applications [23].

The Lab-STICC/CACS team has a strong background in the domain of error control code and the development of signal processing architecture (Lab-STICC/CACS provided complex VHDL cores to several companies in a frame of private contracts). In 2009, Lab-STICC/CACS starts to investigate the domain of computing on unreliable hardware in collaboration of Chris Winstead (PhD of Yangyang Tang [11], [24], [25], [12]). Moreover, our over-Atlantic partner, Prof. Chris Winstead is head of the Low Energy, Fault Tolerant Lab of Utah-State University (`http://left.usu.edu/lab/`). He has several contributions in the field: among which, a seminal paper on stochastic iterative decoder [26] and the proposition of a modified C-Muller structure for Triple Modular Redundancy architecture [27]. Finally, stochastic implementation requires generation of random sequence with a given probability. Lab-STICC has a strong experience in this field [28], [29], and provides also in VHDL (langage for hardware description) a free random gaussian noise generators (see `http://www-labsticc.univ-ubs.fr/~boutillon/wgng/wgng.html`, download several hundred of times worldwide).

2.3 WP3: Study on error sensibility

WP3 is lead by Emmanuel Casseau, from IRISA-Cairn.

2.3.1 Task description

This task is devoted to methods and tools for the evaluation of errors effects on hardware computing units. We will focus on simple and advanced arithmetic operators (including their control resources). We propose to work on 2 complementary sub-tasks:

- theoretical analysis for modeling the fault impact on arithmetic circuits,
- FPGA emulation techniques for an empirical but accurate evaluation of fault impact in arithmetic circuits.

In the first sub-task, we will study the impact of faults in arithmetic circuits using analytical models. The behavior of arithmetic computations is usually characterized by accuracy models or estimations. Two kinds of accuracy models are used to evaluate the impact of general errors in arithmetic computations: average errors and worst case errors. In the case of average errors, the mathematical errors are considered as an additional noise independent from the operands. For this type of error analysis, several solutions have been developed such as for fixed-point arithmetic. In the case of worst case errors, the errors are linked to the operands (e.g. bit flipping in the most significant bits). This kind of errors better covers the scope of the project. Previous works only focused on the propagation of mathematical errors in the input data through the operators. This well known type of error propagation corresponds to a functional behavior that does not depend on the algorithms and their physical implementation. In this project, the errors we target are due to physical faults and can not only be seen as a mathematical noise on the inputs. They can be seen as failures of the logical description in the operators (they can occur in the data part as well as in the control part of the implemented algorithm). We propose to try to model the behavior of arithmetic operators in the presence of some fault models (bit flip, stuck at, one digit or several digits, etc.) based on WP1. Our main objective is to propose accuracy models for various fault models, algorithms and implementation styles. This would guide design choices in the WP4. In a first time, we will work on basic operators (adders/subtracters, multipliers) and basic representations (2's complement integers and fixed-point). In a second time, we will try to study more complex operators (e.g. sums/accumulation of products, division, reciprocal, square root, polynomial approximations) and representations of numbers used in WP2.

In the second sub-task, we will experimentally study and measure the fault impact on a large library of arithmetic operators for various representations of numbers and fault models. Actually, VHDL simulations can be used but they are very slow. We propose to use FPGA emulation (Field Programmable Gate Array) that is several orders of magnitude faster than software simulation. Each evaluated operator (for each variant, based on techniques proposed in WP2) will be synthesized on a fast FPGA circuit with an embedded fault injection system also emulated in the FPGA. The original description of the operator will be modified with several fault injection points (bit flips, stuck at). This modified description will be implemented on the FPGA alongside an instance of the original version (without fault injection) of the operator. Their results will be compared to accurately measure the fault detection and tolerance characteristics (average rates, distribution). Several scenarios for fault injection will be defined and tested for a huge number of test values at the speed of the FPGA. The objective is to get very accurate statistical results (with narrow confidence intervals). IRISA Lab. has already used this type of FPGA emulation for the evaluation of protection schemes against fault injection attacks in arithmetic operators for elliptic curve cryptography [30] and for power estimation in multipliers [31, 32]. For the Reliasic project we will have to adapt our fault injectors (designed to model cryptographic attacks and power estimation) to the fault models proposed in the WP1.

2.3.2 Interaction with others work packages

In WP2, methods for hardening the computations will be investigated. The impact of these methods will have to be evaluated. It is the goal of WP3. WP3 and WP2 will thus work jointly. First WP3 sub-task will try to evaluate the impact of WP2 methods based on analytical approaches whereas the second sub-task will use emulation to measure fault detection/tolerance capabilities. WP3 is also deeply connected with WP1. Actually, the errors we address must be modeled. This will be done in WP1. The error models will then be used in WP3. Finally, WP3 will provide fault detection/protection models that will be used in WP4 to evaluate the overall behavior of the

application . To summarise, both WP1 and WP2 can be considered as inputs of WP3 whereas WP3 will be an input for WP4.

2.3.3 WP organization and resources

IRISA:

- Emmanuel Casseau, Prof. UR1, Arnaud Tisserand, CR CNRS
- 1 PhD student (1/2 time)
- 1 Master student (6 months)

Lab-STICC/CACS:

- Emmanuel Boutillon, Prof. UBS, Jean-Philippe Diguet, DR, CNRS

IETR/SCN:

- Olivier Pasquier (assistant prof., Polytech Nantes), Sébastien Pillement (assistant Prof., Polytech Nantes)

To achieve the FPGA-based emulation sub-task, we will buy two recent FPGA cards equipped with a large Zynq 7 FPGA circuit (3000 Euros per card). One card will be used by the PhD student, the second one by the permanent researchers and the master students. This FPGA emulation platform will be used to evaluate the quality of the techniques proposed in the WP2.

2.3.4 Partner skills and background

IRISA-Cairn team has a strong background in the domain of evaluation of range bound and arithmetic accuracy using analytical methods and published more than 7 journal papers and 22 conference papers in this topic. Several approaches have been proposed, [33] and [34] among recent ones, and a tool framework is also available (`http://idfix.gforge.inria.fr`). The team also developed tools for the evaluation of the arithmetic worst case accuracy in integrated circuits [35] and modeled accuracy for the automatic generation of arithmetic operators [36]. IRISA-Cairn team also evaluated the impact of redundant signed digit number systems on the security of arithmetic operators for cryptography (on elliptic curves) with respect to fault injection [30]. The team also experiment FPGA-based emulation for the evaluation of activity in cryptographic circuits [32].

Lab-STICC/CACS team has an strong background in the area of trade-off between performance and complexity. Lab-STICC proposes several methods in the frame of error control decoder architecture and signal processing ([37], [38], [39]). in a joint NSF-CNRS project. This project gave several journal publications.

2.4 WP4: Integration of reliability in the design process

WP2 is lead by Sébastien Pillement, from IETR/SCN (Polytech Nantes).

As mentioned above, the targeted application of the project can support different functioning modes. We can then consider several strategies of detection/correction [40] depending on the accuracy targeted for the system, even in the presence of faults in it (different from input faults). All these strategies add functions in the developed component and imply a specific way to handle inputs and internal signals increasing the system complexity. According to the application

requirements (in terms of performance and accuracy) and to the numerous solutions of protection we have to drive the chip designer to the best solution achievable. This WP aims at defining a methodology supporting the design of reliable applications on unreliable silicon. In this project we will focus on the optimization of the reliability and energy efficiency trade-off. This trade-off will be evaluated according to the application constraints.

The proposed methodology would be used to help the designer to model and develop viable options/scenarios using the specific operators (and arithmetic's) developed in the WP2. This design framework will use the evaluation of the fault impact driven in the WP3 and aims at defining the combination rules of the related properties of the different solutions in order to propose the best compromise between reliability and power-consumption. The models used during this process will help to evaluate the potential benefits of using a particular approach before the completion of the circuit on silicon by providing information to compare the different solutions.

To setup the complete methodology this WP is divided in three tasks.

1. Application Constraints model

   This first task will consist in developing constraints models from the specifications of the targeted application. The model should include the performance requirements capture according to reliability and possible degradation of accuracy of the application. For example in the GPS application proposed in this project we expect to represent that (for example) the protected version of the application should not increase the mean TFF (Time to First Fix) of about 20%, or the protected version of the design should not provide a positioning error superior to 2km compared to the unprotected version.

   These constraints and requirements will be abstracted, generalized and quantified in terms of expected QoS (energy consumption, accuracy, processing time, respect of deadlines, etc). They will be taken into account as a first entry of the design methodology.

2. Architectural Model

   The proposed methodology should rely on the evaluation of both achievable reliability and energy consumption at the architecture level. This task will aim at evaluating and proposing methods in order to evaluate at an early stage of the design flow the costs overhead of a specific solution to solve the reliability problem. This will help the designers in setting up the required trade-off between reliability and energy efficiency of the system. In this task the relationship of the different models (reliability, energy, application, architecture) involved should be made explicit and evaluated. For example the evolution of the energy overhead should be evaluated according to the particular protection approach used in order to abstract the fundamental information of the underlying hardware. This work will permit to optimize in-fine the final solution and to compare different solutions. These methods and relationship will be another entry point of the methodology and will allow the designer to explore rapidly design choices prior any final implementation on silicon in the WP5.

3. Implementation (Deployment)

   This task will consist in deploying the methodology on the targeted application as a proof of concept. The models and methods that will be developed in the two previous tasks will be used and implemented in this task. For that purpose specific meta-models or domain-specific-language should be used in order to generalize the proposed approaches. The models transformations should be formalized aiming at implementing tools for increasing the design efficiency. The methodology deployment should be validated thanks to the GPS application used in the project.

2.4.1 Interaction with others work packages

This WP is directly linked with WP3, which will allow the identification and evaluation of the sensitivity of different operators and should be strongly coupled with the methodology, to guide the design towards a realistic solution. The futures techniques proposed in WP2 will be added as new options for fault mitigations in the design flow. Comparing the evaluations done using the proposed models with the characteristics obtained in the WP5 circuits will do the validation of this WP.

2.4.2 WP organization and resources

IETR:

- Sébastien Pillement PR UN, Olivier Pasquier McF UN, Jean-Christophe Prevotet McF INSA
- 1 PhD student
- 2 M2R students

Lab-STICC(UBO):

- Catherine Dezan (assistant professor).

2.4.3 Partner skills and background

The SCN team has strong achievement in embedded system design methodology definition [41]. Previous works [42] on this domain leads to the creation of the CoFluent Company, which now belongs to Intel. We have skills in the design of fault tolerant circuits using different strategies (use of specific coding [43], or dedicated approach such as dynamic reconfiguration [44]). The SCN team is leader of the ANR ARDyT project (`http://ardyt.irisa.fr/`) in the field of designing low-cost reliability mechanisms for a reconfigurable architecture. The architecture development aspects of the team use our proficiency in designing and implementing low-power signal processing algorithms.

2.5 WP5: ASIC design

WP5 is lead by Cyril Lahuec, from Lab-STICC/MOCS (Telecom Bretagne).

2.5.1 Task description

Task 1: This task involves the on-chip implementation of a circuit implementing two versions of the chosen application. The first one will is straight forward implementation without any fault compensation technique. Therefore place-and-route tools will automatically generate the layout of the circuit. The second one will be compensated for the identified faults using the techniques developed in WP2. A mix of solution might be chosen which will imply some full-custom design to be done. Moreover, it might be interesting to put some test structures directly on chip. T5-1 also includes the design of such structures. Finally, both circuits will be placed on the same chip along with the test structure. This final step is done as in the case of full-custom chip. The chosen technology for implementation is a 28 nm CMOS one.

Deliverables: a dozen of 28 nm CMOS ASICs.

Task 2: Description: the chip designed in T5-1 needs a dedicated test board that will be design and fabricated in T5-2. Then a test-bench will be set-up to assess the functioning of both the uncompensated and compensated application. Selected test vectors will be designed and used to assess the performance of each circuit as the voltage supply is decreased and as the chip suffers noise. The chips will also be tested for functionality versus temperature and process variations, as lowering the supply voltage makes the devices more sensitive to these parameters.

Deliverables: a test report.

2.5.2 Interaction with others work packages

The VHDL files will be delivered by WP2. Then, in the last year of the project, the measurements done in WP5 will be used to test, validate and improve the models of WP1, WP2, WP3 and WP4.

2.5.3 WP organisation and resources

IETR:

- Jean-Christophe Prevotet, Assistant Prof., INSA-Rennes.

Lab-STICC:

- Fabrice Seguin, Assistant Prof. TB, Cyril Lahuec, Assistant Prof. TB.
- Emmanuel Boutillon, Prof. UBS.
- Chris Winstead, Prof. Utah State University.
- 1 senior engineer for the backend operation of the ASIC design (12 months).

Moreover, 40k€will be used for the direct cost fabrication of the ASIC.

2.5.4 Partners skills

The researchers involved in this work package have experience in IC design and test. They made a dozen full custom integrated for applications ranging from radio frequencies to channel decoding circuit. [45–52] including low power sub-threshold CMOS circuits [53]

Chapter 3

Partners description

3.1 IETR/SCN

The bi-localized SCN team of the IETR lab has extensive expertise on methodology and modelling for the design of embedded circuits and digital communications systems. The strength of the team is to bring together expertise from both architecture and signal processing communities. This mix of skills allows us to develop new and innovative approaches for optimization of advanced algorithms and implementation of complex platforms. The SCN research team relies on its expertise and considers since many years multiples constraints in its designs such as dependability and energy consumption. The team also has extensive experience in the development and design of prototyping platforms implementing proof of concept. We currently have two PhD thesis about energy modeling aspects for the design of embedded system and the signal processing chains. In the past we have worked on coding approaches and integration of specific mechanisms to improve fault tolerance in embedded (eg in the automotive domain) systems. This work has given rise to national collaborations and several PhD thesis. In addition the team leads the ANR project ARDyT wherein, in collaboration with the Lab-STICC, IRISA, IJL and ATMEL partners, we develop a fault-tolerant and low cost reconfigurable architecture.

Name	Laboratory	University	Task
O. Pasquier	IETR	Polytech Nantes	involved in WP3 and WP4
S. Pillement	IETR	Polytech Nantes	Leader of WP4, involved in WP3
J.C. Prevotet	IETR	INSA Rennes	involved in WP4 and WP5

Table 3.1: Main researchers of IETR-SCN involved in RELIASIC

Sebastien Pillement is a Professor in Polytech'Nantes, France since 2012. He was an associate professor at IUT in Lannion, the subdivision of the University of Rennes 1, during 13 years. He is currently a member of the SCN Research Team of the IETR Lab. (Research Institute in Electronic and Telecommunication). He received a Ph.D. degree and Habilitation degrees in Computer Science respectively from the University of Montpellier II and the University of Rennes 1. His research interests include dynamically reconfigurable architectures, system on chips, design methodology and NoC (Network on Chip) based circuits. He focuses his research on designing flexible and efficient architectures managed in real-time and on the use of these architectures to increase the reliability of systems. He is the author or coauthor of about 100 journal and conference papers.
`http://pillement.polytech.univ-nantes.fr/`

Olivier Pasquier received the engineering degree in Electronic System Engineering from IRESTE engineer school (Nantes, France) in 1989. He received the PHD degree in Engineer Sci-

ences from IRESTE in 1994. This degree has been prepared in Electronic System Design Methodology Lab. Actually he is an assistant professor in Institute of Electronic and Telecommunication of Rennes (IETR) and he teaches embedded and real-time systems technology and design in Polytech'Nantes engineer school. His research topic deals with Embedded System Design Modeling and Methodology. He is working on high abstraction level modeling of embedded system in order to consider power consumption, safety and reliability early in the design process of embedded systems.

Jean-Christophe Prévotet (assistant professor) joined the IETR (Electronics and Telecommunications Institute of Rennes) in 2007. His major research interests include reconfigurable architecture design and hardware implementation of complex systems. He also has experience in designing heterogeneous SoC platforms (software + hardware) from systems to circuits. His major field of applications concerns Real Time Operating Systems, telecommunication, signal and image processing.

3.2 Lab-STICC

The CACS (Communications, Algorithms, Circuits and Systems) group of the Lab-STICC laboratory (Laboratoire des Sciences et Techniques de lInformation, de la Communication et de la Connaissance) develops effective telecommunication systems for transmission and reception (channel coding, space-time processing, equalization, detection, synchronization ...), based on a joint algorithms and micro-electronics approach, and progress on implementation methods and tools. Its activities constitute a reference in communication system research in both hardware and software aspects.

The IAS (Interaction Algorithm Architecture) section of the CACS is dedicated to the interaction of the know-how in algorithms and circuit design. The development of new algorithms for digital communication and original architectures (analog and digital) for digital communication circuits are the main activities the IAS. One of the most known historical achievements of the IAS was the invention of Turbo Codes by Claude Berrou 20 years ago. This invention was a real revolution in the digital communication field and the IAS benefits from this international recognition, having received several prices such as the Hamming Medal (IEEE), the Marconi Prize, among others. Lab-STICC has recently received and ERC fellow grant about Neural Coding. Neural coding can perform information processing and is, by construction, robust to hardware error. Finally, Lab-STICC has several patents on error code adopted in standards and/or licensed to private companies.

Name	Laboratory	University	Task
E. Boutillon	Lab-STICC	UBS	Project leader, leader of WP2, involved in WP3 and WP5
C. Dezan	Lab-STICC	UBO	involved in WP4
J.P. Diguet	Lab-STICC	UBS	involved in WP2 and WP3
C. Lahuec	Lab-STICC	Telecom B.	Leader of WP5, involved in WP1
F. Seguin	Lab-STICC	Telecom B.	Leader of WP1, involved in WP5
C. Winstead	Lab-STICC	Utah State Univ.	Involved in WP1, WP2 and WP5

Table 3.2: Main resarchers of Lab-STICC (or connected to Lab-STICC) involved in RELIASIC

Emmanuel Boutillon is a professor at the Universite de Bretagne Sud, Lorient. He was the head of the LESTER laboratory from 2005 to 2007 and, since 2008, in charge of the CACS (Communication, Architecture, Circuits and Systems) department of the Lab-STICC. His current research interests are on the interactions between algorithm and architecture in the field of Turbo Codes and LDPC decoders for wireless communications. He published more than 22 journals and 53 international conferences papers and 5 licenced patents. He is senior IEEE member and was

member of the IEEE DISPS committee from 2004 to 2012. He is also member of the CoNRS (National French Committee for Scientific Research).
http://www-labsticc.univ-ubs.fr/~boutillon/anglais.html

J-Philippe Diguet is research director at CNRS and head of the MOCS team at Lab-STICC. He obtained his Ph.D degree from Rennes University in 1996, he has been a visitor researcher at IMEC in 1997 and then associated professor at UBS University from 1998 until 2002. In 2003, he was involved in a technology transfer in the domain of wireless embedded systems. Since 2004 he is a CNRS researcher at Lab-STICC. He has been a visitor researcher at the University of Queensland in 2010. His current work focus on various topics in the domain of embedded system design: heterogeneous MPSoC and NoC synthesis, hardware-secured architectures, self-adaptive HW/SW architectures targeting energy efficiency (e.g. body area network) and more recently reliability auto-evaluation in the context of UAV.
http://www-labsticc.univ-ubs.fr/~diguet/

Fabrice Seguin was born in Talence, FRANCE in 1973. He received the Ph.D. degree from the Universite Bordeaux 1, France, in 2001. His doctoral research concerned the current mode design of high-speed current-conveyors and applications in RF circuits. In 2002, he joined the Electronic Engineering Department of Telecom Bretagne, Brest, France, as a full-time lecturer. At PRACOM, (Ple de Recherche Avanc/'e en Communications) he is involved with design issues of analogue channel decoders and related topics, Energy harvesting, neural coding, and reliability in nanoscale technology.
https://perso.telecom-bretagne.eu/fabriceseguin/

Cyril Lahuec was born in Orleans, France, in 1972. He received the B.Sc (Hon.) degree from the University of Central Lancashire (UK) in 1993, his M.Eng (mode A, by research) and Ph.D degrees from Cork Institute of Technology (Ireland) in 1999 and 2002, respectively. Finally, he received the "Habilitation a Diriger des Recherches" form the Universitée de Bretagne Sud" in June 2012. He was with Parthus Technologies (now Ceva) Cork for his Ph.D work and then as a consultant. He joined the Department of Electronic Engineering of TELECOM Bretagne as a full-time lecturer in 2002. He was with the CMOS Sensors & Systems group at the University of Edinburgh as a Visiting Researcher for 4 months in 2011. His research interests are in frequency synthesis, analogue IC design, channel decoding and biomedical applications, leading to the design and fabrication of a dozen full-custom CMOS/BiCMOS chips.
https://perso.telecom-bretagne.eu/cyrillahuec/

Catherine Dezan received the engineering degree from the Ecole Nationale Suprieure des Tlcommunications de Bretagne (Brest, France) in 1989 and the Ph.D degree in Computer Science from the Universit de Rennes I (France) in 1993. Since 1994, she has been an Associate Professor at the Universit de Bretagne Occidentale (Brest) in Computer Science. In 2006-2007, she spent one year as invited professor at the University of Massachusetts (USA), and worked with Prof. Moritz on nanoscale architectures and on fault tolerance mechanisms. Her main interests are on design methodologies/tools and applications for hardware implementations with a special focus on parallel, reconfigurable and nanoscale architectures.
http://pagesperso.univ-brest.fr/~dezan

Chris Winstead received the B.S. degree in Electrical and Computer Engineering from the University of Utah in 2000, and the Ph.D. degree from the University of Alberta in 2005. He is currently with the ECE Department at Utah State University, where he holds the rank of Associate Professor. Dr. Winstead's research interests include low-power and fault-tolerant VLSI circuits, implementation of error-correction algorithms, modeling and design principles for stochastic circuits in electronics and synthetic biology, and mixed-signal design for reliable wireless communication. He has authored more than 40 technical articles, and in 2010 he received the Career Award from the US National Science Foundation. Dr. Winstead is a Senior Member of the IEEE and is a member of the Tau Beta Pi engineering honor society. In 2012, he received a Fulbright grant for its sabbatical year in the University of Bretagne Sud.
http://www.neng.usu.edu/ece/faculty/winstead/

3.3 IRISA-Cairn

IRISA-Cairn team is a joint research project-team associated to INRIA, CNRS, UR1 and ENS Cachan. IRISA-Cairns members are recognized for their expertise in the fields of energy-efficient system-on-chips and reconfigurable architectures, signal processing and computer arithmetic for mobile communications, cryptography and wireless sensor networks. The IRISA-Cairn team has participated in several National and European Research & Development projects and has strong industrial collaborations (e.g. Thales, Alcatel, Orange, STMicroelectronics, Thomson and various SMEs). IRISA-Cairn has some recognized expertise on hardware architectures, circuit design, CAD tools and embedded software.

Name	Laboratory	University	Task
E. Casseau	IRISA-Cairn	Rennes 1	Leader of WP3, involved in WP2
A. Tisserand	IRISA-Cairn	CNRS	involved in WP3 and WP2

Table 3.3: Main researchers of IRISA-Cairn involved in RELIASIC

Emmanuel Casseau received the M.S. degree in Electrical Engineering in 1990 and the Ph.D degree in Electrical and Computer Engineering from the Universite de Bretagne Ouest, France, in 1994. From 1994 to 1996 he was a research engineer in the French National Telecom School, ENST Bretagne, France. From 1996 to 2006 he was an Associate Professor in the Electronic Department at the Universite de Bretagne Sud, France. He is currently a Professor in IRISA Lab., Cairn team in Lannion, Universite de Rennes 1, France. His research interests include VLSI design, SoCs design methodologies and reconfigurable architectures for video processing applications.
`http://perso.univ-rennes1.fr/emmanuel.casseau/`

Arnaud Tisserand received the M.S. degree in 1994 and the Ph.D. degree in 1997 both in Computer Science from the (*École Normale Supérieure de Lyon*), and the HDR degree (*Habilitation à Diriger des Recherches*) in Computer Science in 2010 from the University of Rennes. From 1997 to 2005, he was INRIA researcher at LIP laboratory in Lyon. From 2005 to 2008, he was CNRS researcher and former head of the ARITH research group at LIRMM laboratory in Montpellier. Since 2008, he is CNRS researcher (CR1) at IRISA laboratory, CAIRN team, in Lannion. His research interests include computer arithmetic (computation algorithms and representations of numbers), circuit design on ASICs and FPGAs, fault tolerant circuits and low-power design for applications in scientific computing, digital signal processing and cryptography.
`http://people.irisa.fr/Arnaud.Tisserand/`

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