IEEE International Symposium on Circuits and Systems, ISCAS 2012, COEX, Seoul, Korea, 20-23, May, 2012

An LDPC Decoding Method for Fault-Tolerant Digital Logic





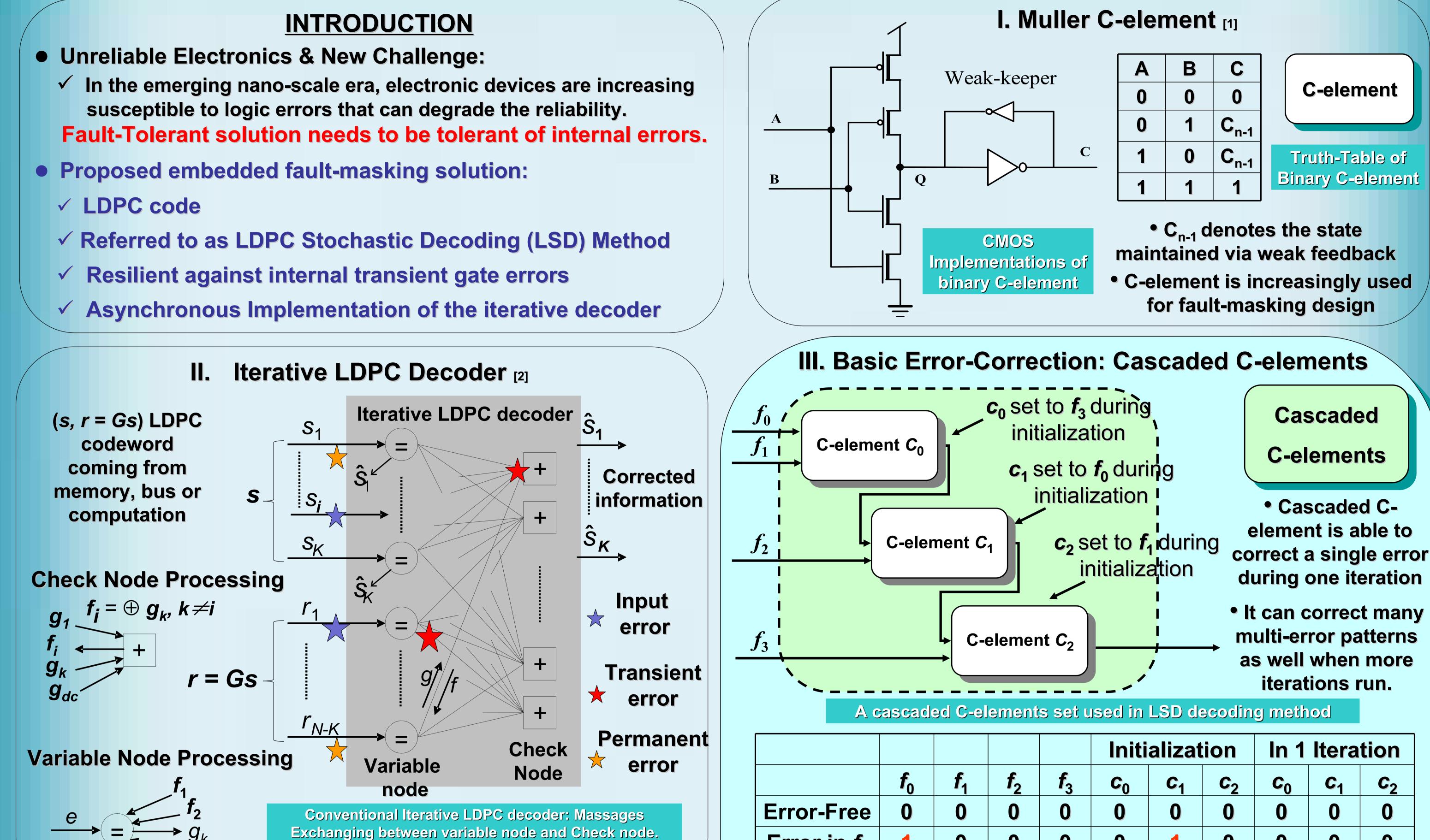
Yangyang Tang^{1,2}, Chris Winstead², Emanuel Boutilon¹, Christophe Jégo² and Michel Jézéquel³

¹Université de Bretagne Sud, UMR CNRS 6285 Lab-STICC, Lorient, France ²Dept. of Electrical and Computer Engineering, Utah State University, Logan, Utah 84322 ³Institut Polytechnique Bordeaux, UMR CNRS 5218 Lab-IMS, Bordeaux, France ⁴Institut TELECOM/TELECOM Bretagne, UMR CNRS 6285 Lab-STICC, Brest, France yangyang.tang@univ-ubs.fr



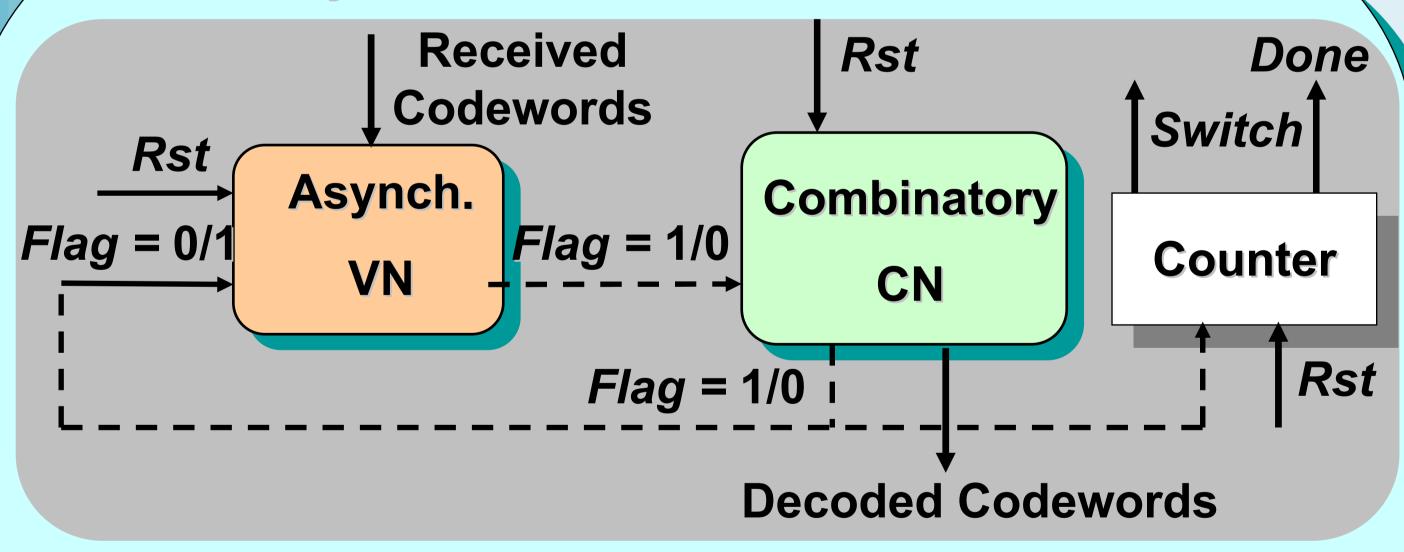


- - ✓ In the emerging nano-scale era, electronic devices are increasing susceptible to logic errors that can degrade the reliability.



$\neg f_{dv}$ $g_k = e \text{ if } (f_i, i \neq k) \text{ disagree, } f_1 \text{ elsewise}$

IV. Asynchronous Architecture of the LSD



Asynchronous Handshaking Signal Flow of the LSD Architecture

• LSD's Error-Correction Steps:

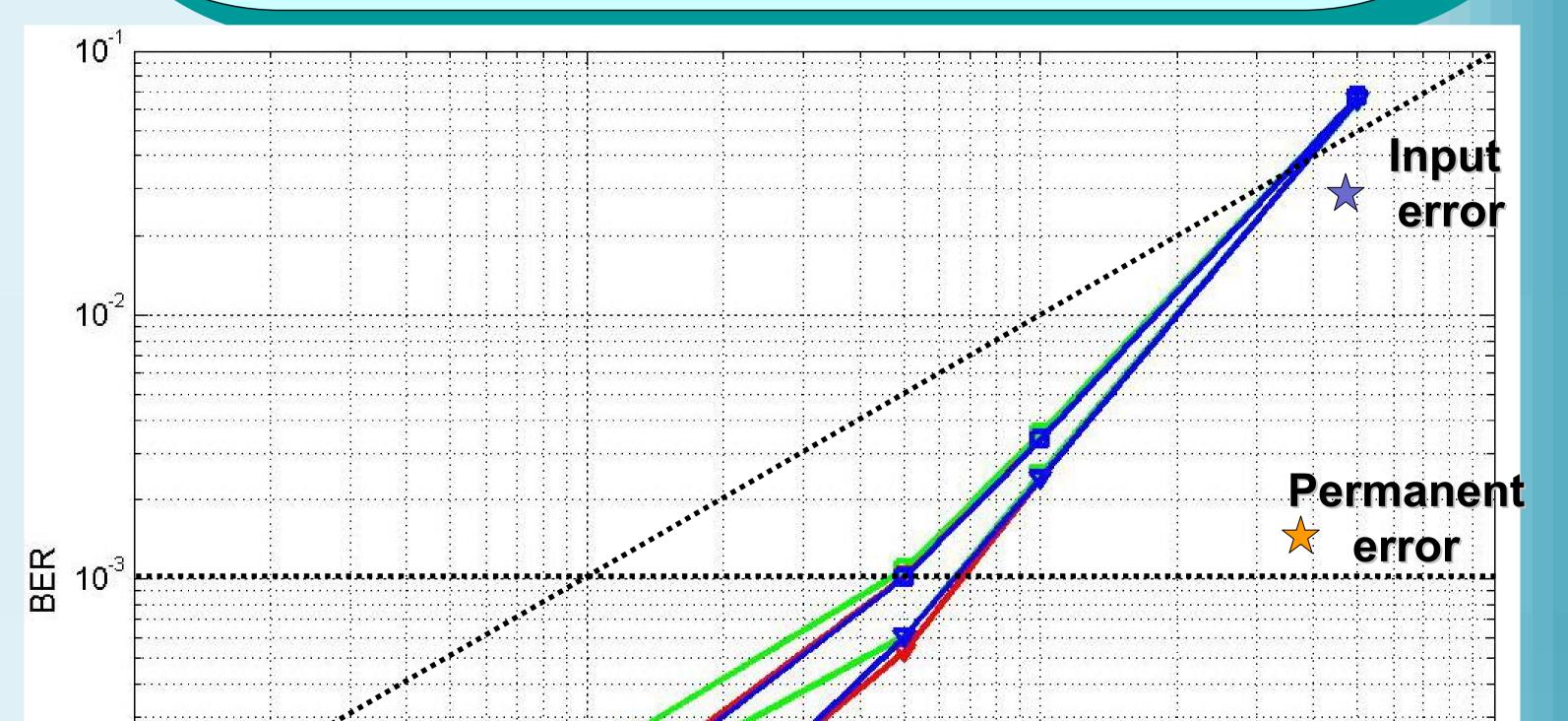
Initialization Phase:

- 1: Modulo-2 summation in XORs for the received codewords.
- 2: Cascaded C-elements initialize the memories with the incoming messages and perform a basic error-correction.

Error in T_0	1	U	U	U	U	1	U	U	U	U
Error in <i>f</i> ₁	0	1	0	0	0	0	1	0	0	0
Error in <i>f</i> ₂	0	0	1	0	0	0	0	0	0	0
Error in <i>f</i> ₃	0	0	0	1	1	0	0	0	0	0

A Table that illustrates the behaviors of the error-correction

• LSD is a message-passing decoding method [2], where Variable <u>nodes (Cascaded C-elements)</u> and <u>Check nodes (XOR Arrays)</u> perform the message processing for the received codeword.



Error-Correction Phase:

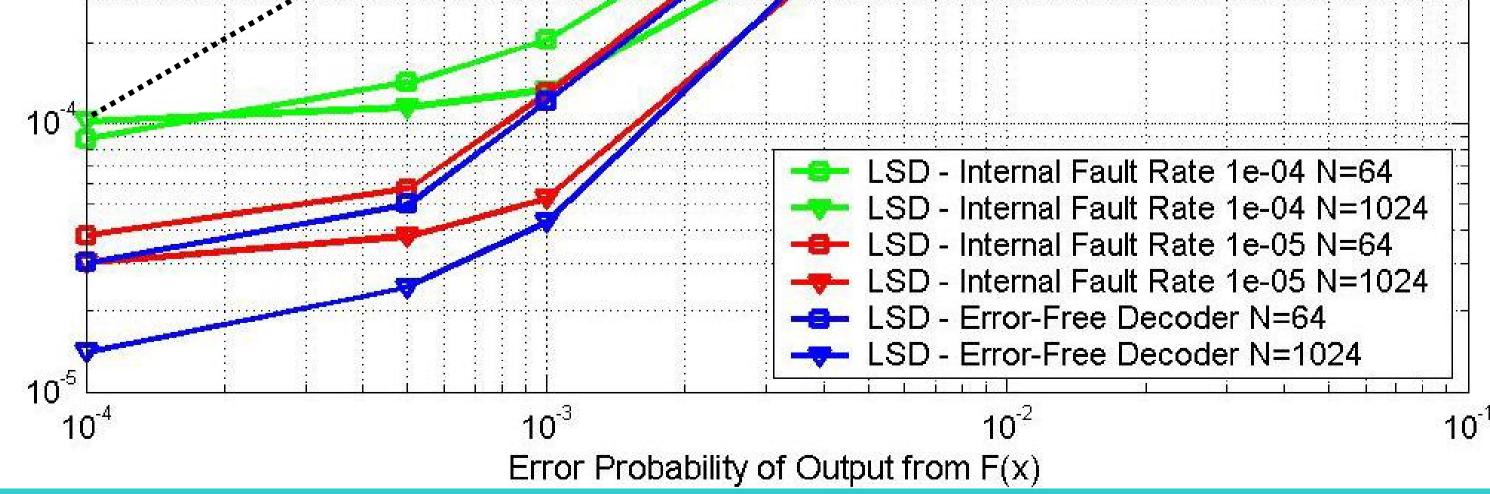
3: Modulo-2 summation in XORs for the massages from C-elements. 4: C-elements perform the error-correction for incoming massages. 5: Iterate step 3 and step 4 during a number of iterations. 6: Output decoded codewords.

Rst: Indicates the decoding phase, *Switch*: to switch the phase, *flag*: signals to control the handshaking protocol.

V. Conclusion

 The originality of LSD method is to implement variable node's computations by C-elements that can resilient against internal faults.

• The LSD approach is able to reduce the error probability at the output of a combinational function by multiple orders of magnitude.



Simulation Results for rate-1/2 (4,8) LDPC codes based on LSD architecture with five iterations. The hard-fault rate for the output from F(x) and E-F(x) is 0.001.

References:

- [1] D.E. Muller and W.S. Bertky, "A theory of asynchronous circuits," in Proc. International Symposium on the Theory of Switching, 1959.
- [2] T.J. Richardson and R.L. Urbanke, "The capacity of low-density parity-check codes under massagepassing decoding," IEEE Transactions on Information Theory, 2001.