Demonstration:
Emulation environment
of a DVB-S2 decoder

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“Interaction Algorithm Architecture” team of Lab-STICC/pole CACS, develops jointly algorithm and associated architecture to optimize overall cost.

For the physical layer, the quality is measured in term of Bit Error Rate (BER) and the complexity in terms of area, time to design and power dissipation.

Optimization is a very complex task since:

- Many parameters to optimize;
- Evaluation of performance requires heavy Monte-Carlo simulations, for example, determining at which level of signal to noise ratio a LDPC decoder architecture is compliant with the DVB-S2 standard requires the simulation of more than 10 000 000 000 000 bits!
Solution developed in the Frame of PALMYRE II

◊ In order to reduce Monte-Carlo simulation, we can:
  ◊ Exploit also the soft information of a Monte-Carlo simulation [1]
  ◊ Reduce the number of Monte-Carlo simulation to be run [2]
  ◊ Speed up the Monte-Carlo simulation, replacing CPU based simulation by FPGA based emulation.

◊ The last item required to emulate also the channel:
  Hardware Discrete Channel Emulator [3].

New idea

- **Straight method:** Direct emulation of the AWGN channel.
  
  \[(\text{Noise } N(0,1))\]  
  
  \[\begin{align*} 
  \begin{array}{c} 
  W \quad 16 \quad \times \quad 16 \\
  O \quad 16 \\
  \end{array} 
  \end{align*}\]

  Quantization \([-R,R], q \text{ bits}\)

- **New method:** emulate channel + quantization.
  
  \[w (\text{Noise } N(0,\sigma))\]

  \[\begin{align*} 
  \begin{array}{c} 
  O \quad x \\
  \end{array} 
  \end{align*}\]

  Quantization \([-R,R], q \text{ bits}\)
DISCRETE HARDWARE CHANNEL EMULATOR

- FOR A GIVEN $x$, $\sigma$ and $R$, $y_Q$ is EQUIVALENT TO A DISCRETE R.V.
Principle of generation of a discrete random variable.

- 1D method
  - Draw a random number between [0,1] and see where it falls

![Discrete random variable with N=4 values, represented by color](image)

- Complex to implement: the value $x$ needs to be compared to all the thresholds ($N-1$ comparisons).

- Solution: go toward 2D.
Principle of generation of a discrete random variable.

- 2D method
  - Principle: generate two random variables $x,y$ between $[0,1]$ and see where they fall.

- No simplification $\Rightarrow$ need a structure.
Principle of generation of a discrete random variable.

- 2D method: with \( x \), select a column, with \( y \), select color 1 or 2 in the column.

- \( X \): random number between 1 to \( N \) to select color 1 (\( c_1 \)), then, read color 2 (\( c_2 \)) and the threshold \( T \) in a memory and compare \( y \) to \( T \) to select \( c_1 \) or \( c_2 \).
Hardware Discrete Channel Emulator.

Uniform noise Generator (Based on LFSR)

Alias method
Coherent set of simulation/emulation

- **User**
- **Host PC**
  - C program for configuration of the hardware
  - VHDL of HDCE
  - VHDL of Coder/decoder
  - C model of HDCE
  - C model of coder/decoder
  - PDF generation
  - Seed management
- **FGPA Board**
  - Hardware emulation
  - Synthesis
  - Netlist

Parameters for hardware synthesis

Simulation results
Application: range of quantization for a LDPC (DVB-S2) decoder

Optimal value of $R$ ?

- $R=0.25 =>$ Saturates most of the time $\Leftrightarrow$ hard decision
- $R=0.9 =>$ Better match
- $R=5 =>$ To much erasure...

- Innovation: using “vertical scheduling” instead of “horizontal scheduling”.
- Size: 64 800 bits, rate ½ and 2/3 (proof of concept).
- Decoding throughput: 200 Mbit/s (information bit) with 36 decoding iterations on a Xilinx Virtex 5.
Scenario of emulation.

User

Range R
SNRs

Code rate
Nb of iterations

Max frame
Max error
Range of SNR

Time

Host PC

HDCE engine

Emulation engine

Alias table

FGPA Board

codeword

FIFO

HDCE

LDPC decoder

Control/
FER/BER

RS232

Index of
Undecoded frame

Soft replay of
undecoded
frame to deep
analyse

Test of
17 280 000 000 000 bits/day

Lab-STICC

CPS

palmyre

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Demonstration...
After few days of simulations...

The graph shows the performance of a rate 2/3 LDPC decoder. The BER (Bit Error Rate) is plotted against $E_s/N_0$, where $E_s$ is the energy per bit and $N_0$ is the noise power density. The graph includes lines for different decoding iterations (it) and their corresponding BER ranges:

- It=50 range 1.5
- It=36 range 1.5
- It=36 range 2.0
- It=25 range 1.65

The range of BER that can be obtained by simulation in a reasonable time is indicated by the red line labeled "std limit." The range of BER that can be obtained by hard emulation in a reasonable time is shown by the other lines.

Change of order!
Conclusion

- Methods to optimized error control code architecture using both simulation and emulation.
- So far, methods applied for:
  - NXP (CIFRE): LDPC DVB-S2 (schedul. horizontal).
  - Orange Labs (private contract): Code cortex
  - ETRI (Private contract): LDPC DVB-S2 (schedul. Vertical)
  - DaVinci (FP7): LDPC Non Binaire.