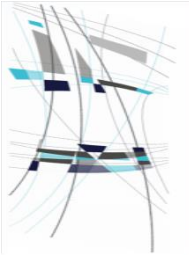




# Demonstration: Emulation environment of a DVB-S2 decoder

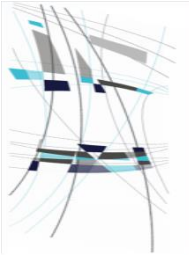
CNRS, UMR 6285, Lab-STICC  
Centre de Recherche - BP 92116  
F-56321 Lorient Cedex - FRANCE





# MOTIVATION

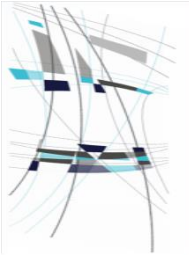
- ◇ “Interaction Algorithm Architecture” team of Lab-STICC/pole CACS, develops jointly algorithm and associated architecture to optimize overall cost.
- ◇ For the physical layer, the quality is measured in term of Bit Error Rate (BER) and the complexity in terms of area, time to design and power dissipation.
- ◇ Optimization is a very complex task since:
  - ◇ Many parameters to optimize;
  - ◇ Evaluation of performance requires heavy Monte-Carlo simulations, for example, determining at which level of signal to noise ratio a LDPC decoder architecture is compliant with the DVB-S2 standard requires the simulation of more than 10 000 000 000 000 bits !



# Solution developed in the Frame of PALMYRE II

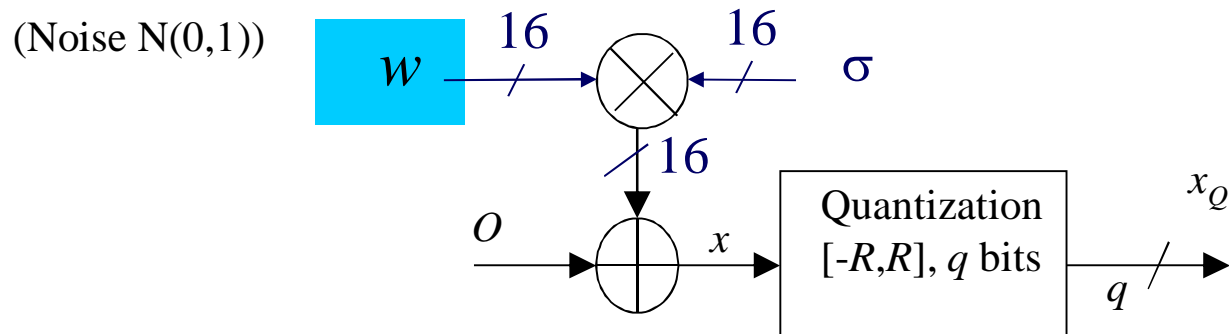
- ◇ In order to reduce Monte-Carlo simulation, we can:
  - ◇ Exploit also the soft information of a Monte-Carlo simulation [1]
  - ◇ Reduce the number of Monte-Carlo simulation to be run [2]
  - ◇ **Speed up the Monte-Carlo simulation, replacing CPU based simulation by FPGA based emulation.**
- ◇ The last item required to emulate also the channel:  
Hardware Discrete Channel Emulator [3].

- [1] A. Singh, A. Al-Ghouwayel, G. Masera, E. Boutillon, "[A New Performance Evaluation Metric for Sub-Optimal Iterative Decoders](#)", IEEE Communications letters, vol. 13, n°7, pp. 513-515, July 2009.
- [2] E. Boutillon, C. Douillard, G. Montorsi, "[Iterative Decoding of Concatenated Convolutional Codes: Implementation Issues](#)", Transactions of the IEEE, vol. 95, n°6, june 2007.
- [3] E. Boutillon, Y. Tang, C. Marchand, P. Bomel, "Hardware Discrete Channel Emulator", The 2010 International Conference on High Performance Computing & Simulation (HPCS 2010), pp 452-458, Caen, June 2010..

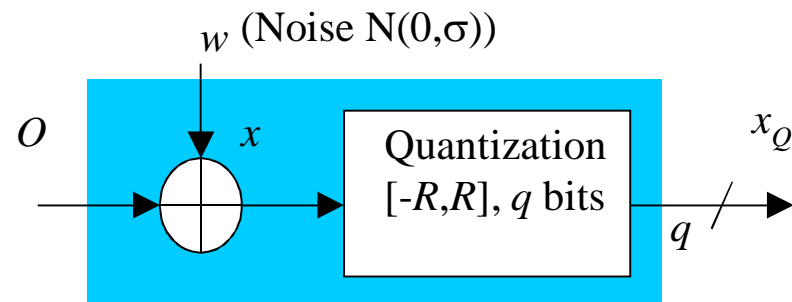


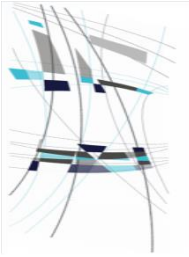
# New idea

- Straight method: Direct emulation of the AWGN channel.

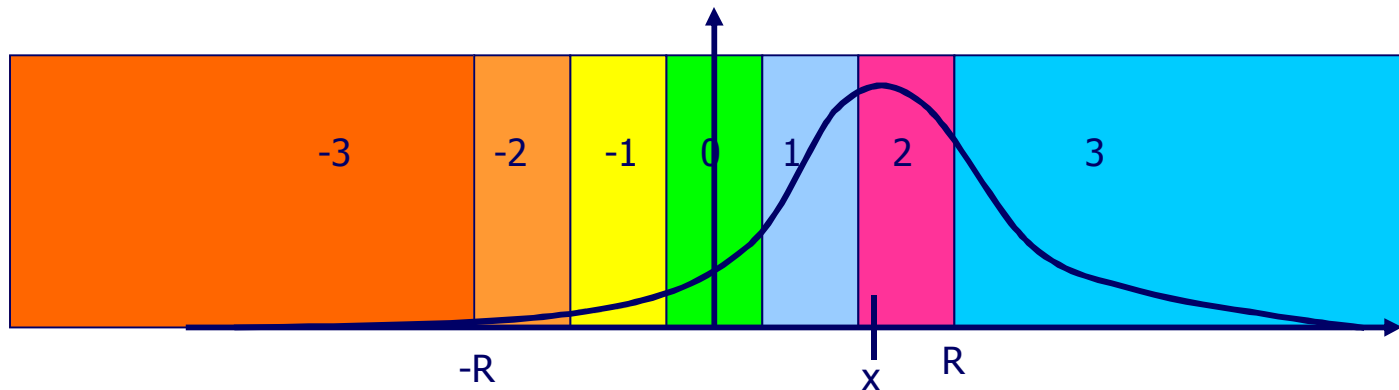
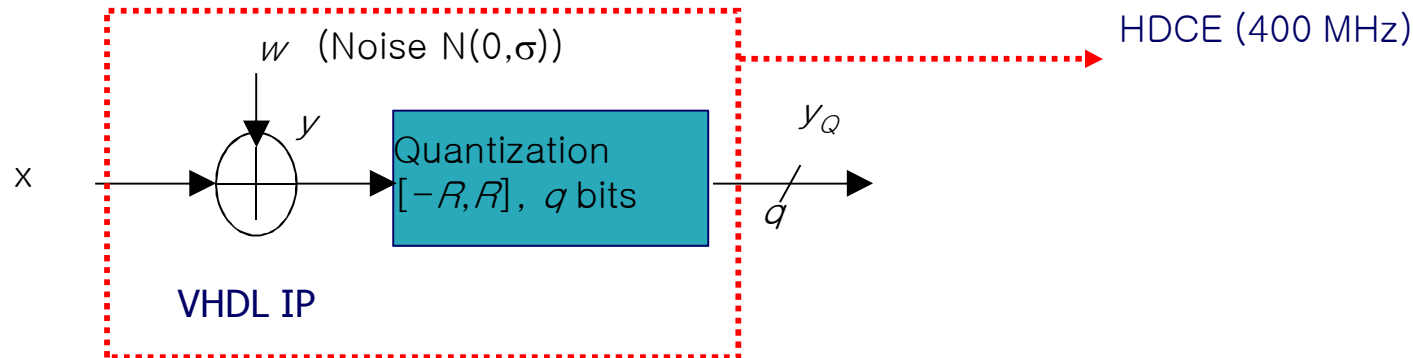


- New method: emulate channel + quantization.

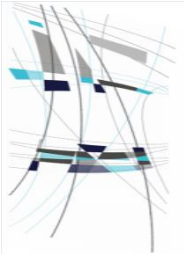




# DISCRETE HARDWARE CHANNEL EMULATOR

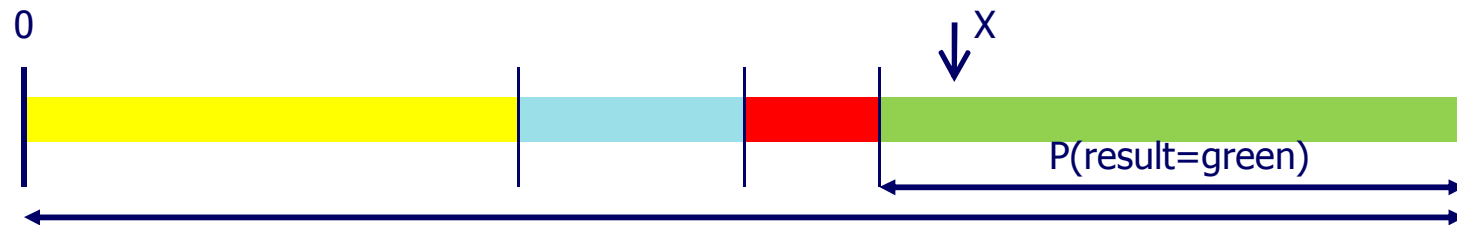


- **FOR A GIVEN  $x$ ,  $\sigma$  and  $R$ ,  $y_q$  is EQUIVALENT TO A DISCRETE R.V.**



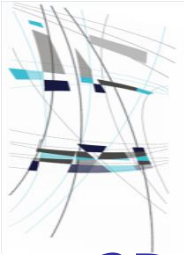
# Principle of generation of a discrete random variable.

- 1D method
  - ◇ Draw a random number between  $[0,1]$  and see where it falls



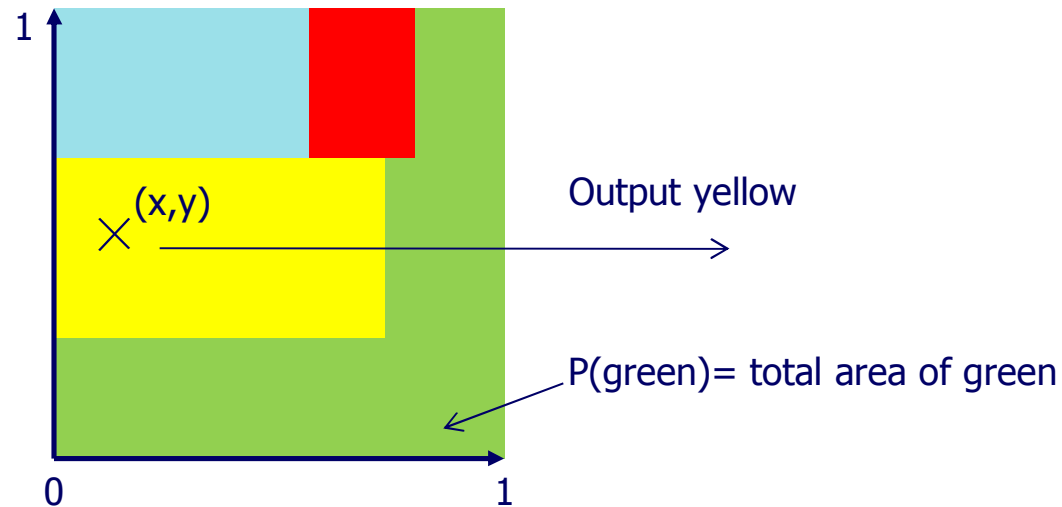
(Discrete random variable with  $N=4$  values, represented by color)

- Complex to implement: the value  $x$  needs to be compared to all the thresholds ( $N-1$  comparisons).
- Solution : go toward 2D.

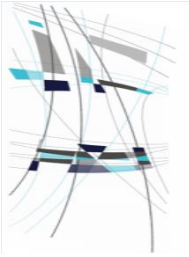


# Principle of generation of a discrete random variable.

- 2D method
  - ◇ Principle: generate two random variables  $x, y$  between  $[0,1]$  and see where they fall.

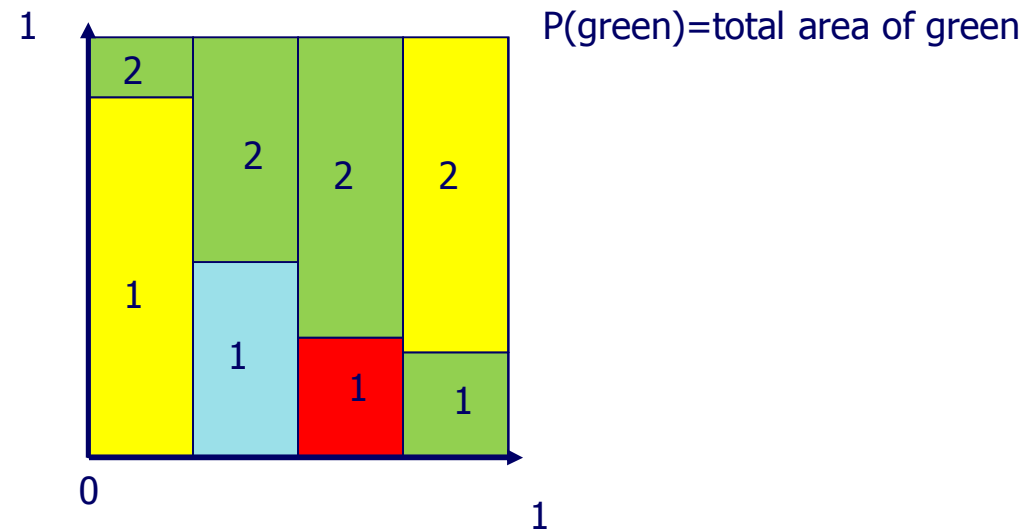


- ◇ No simplification => need a structure.



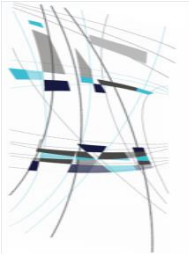
# Principe of generation of a discrete random variable.

- 2D method: with  $x$ , select a column, with  $y$ , select color 1 or 2 in the column.

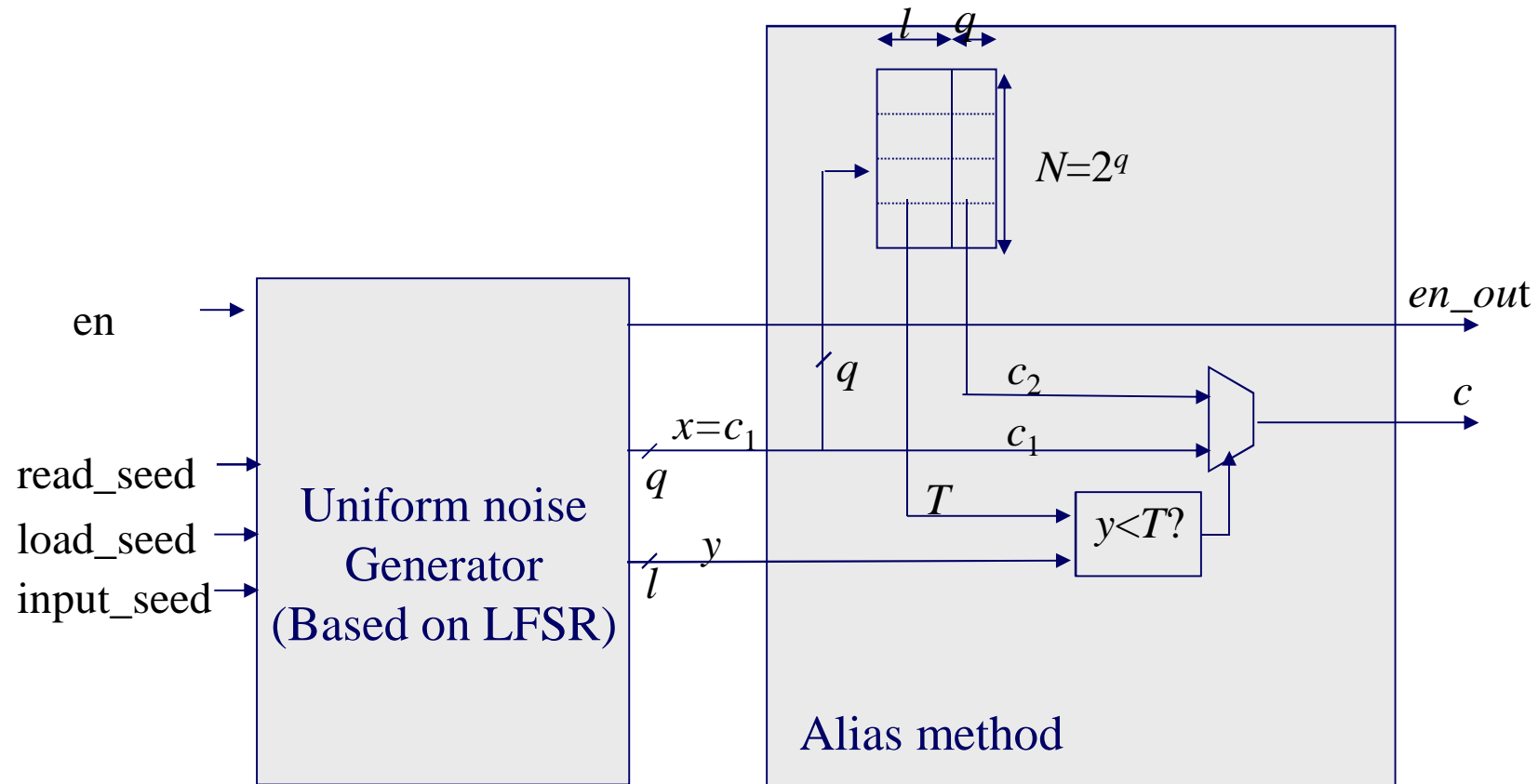


- ◇  $X$ : random number between 1 to  $N$  to select color 1 ( $c_1$ ), then, read color 2 ( $c_2$ ) and the threshold  $T$  in a memory and compare  $y$  to  $T$  to select  $c_1$  or  $c_2$ .

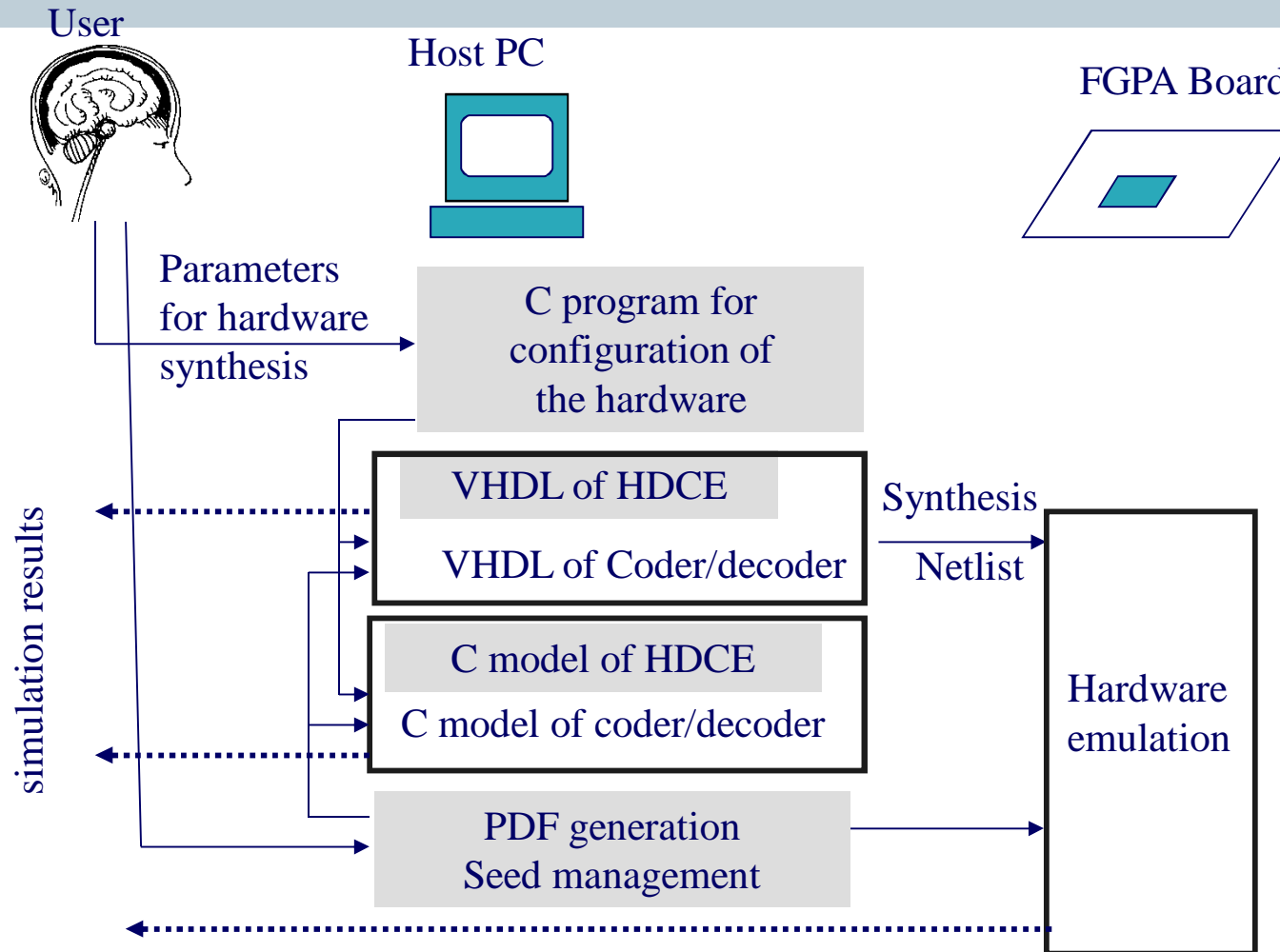


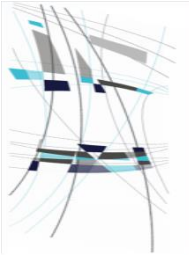


# Hardware Discrete Channel Emulator.

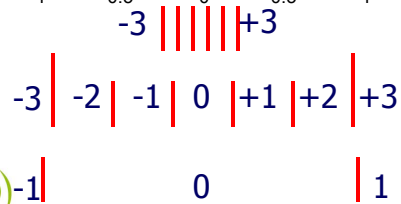
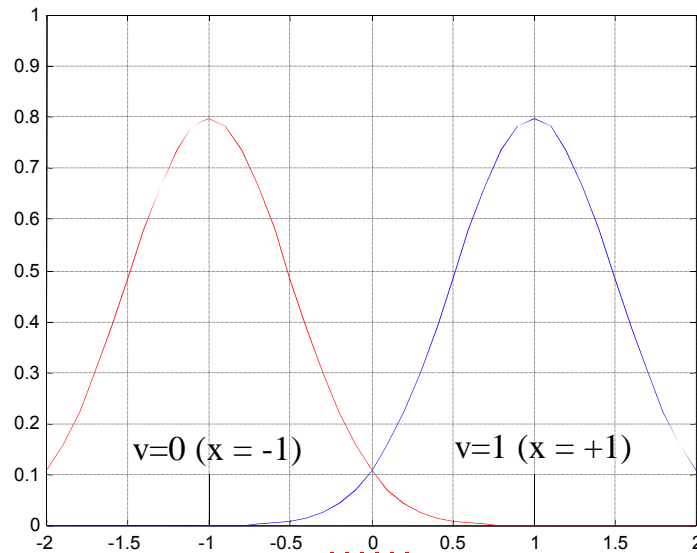
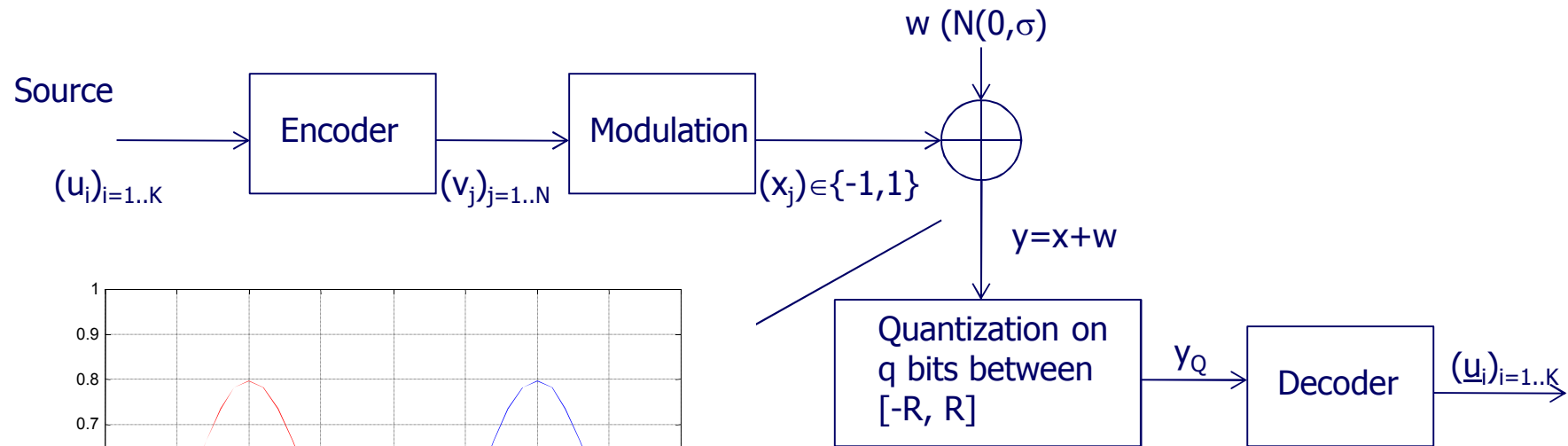


# Coherent set of simulation/emulation





# Application: range of quantization for a LDPC (DVB-S2) decoder

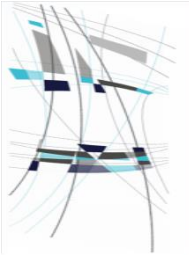


○ Optimal value of R ?

R=0.25 => Saturates most of the time ⇔ hard decision

R=0.9 => Better match

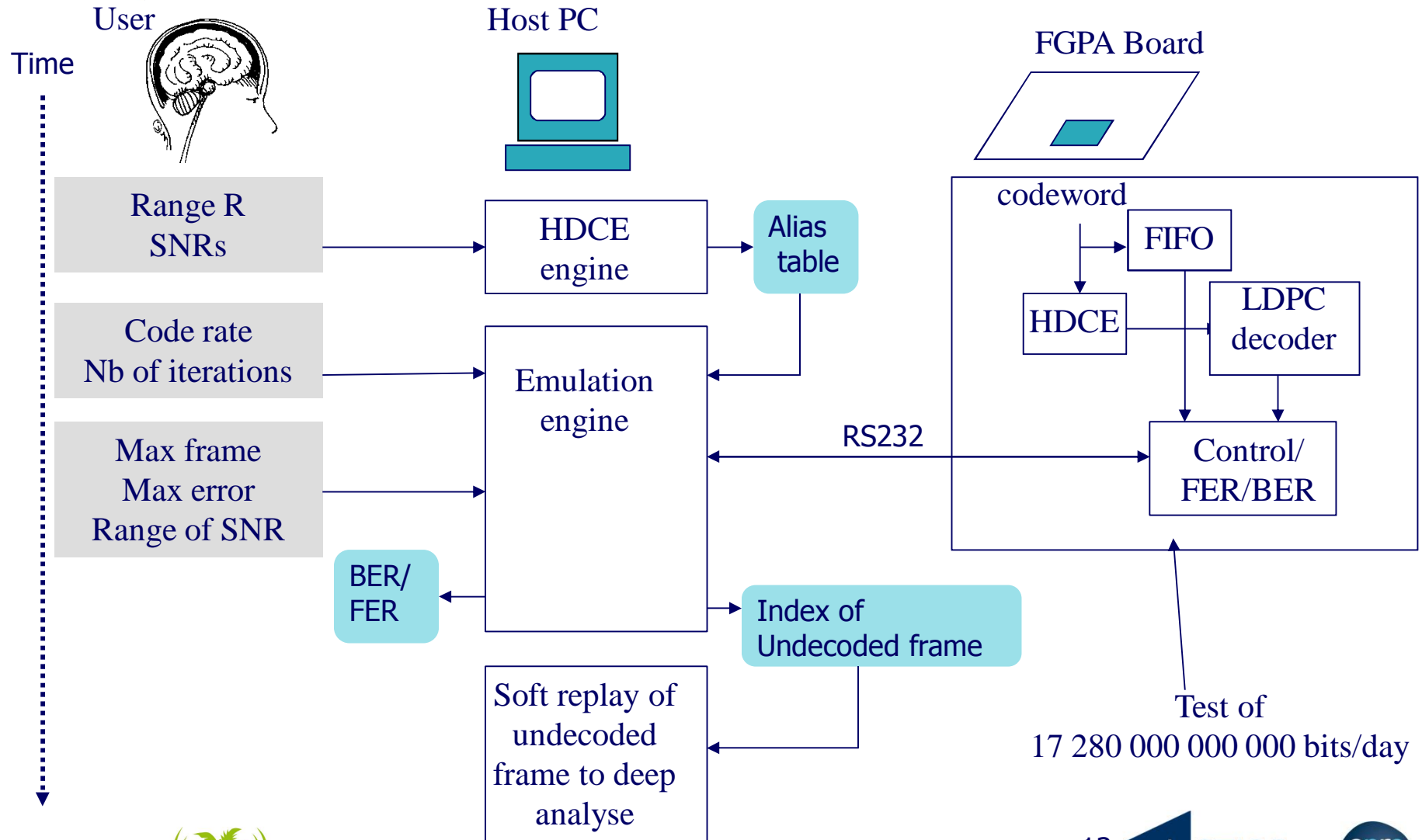
R=5 => To much erasure...

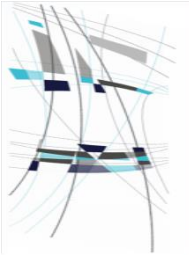


# LDPC decoder

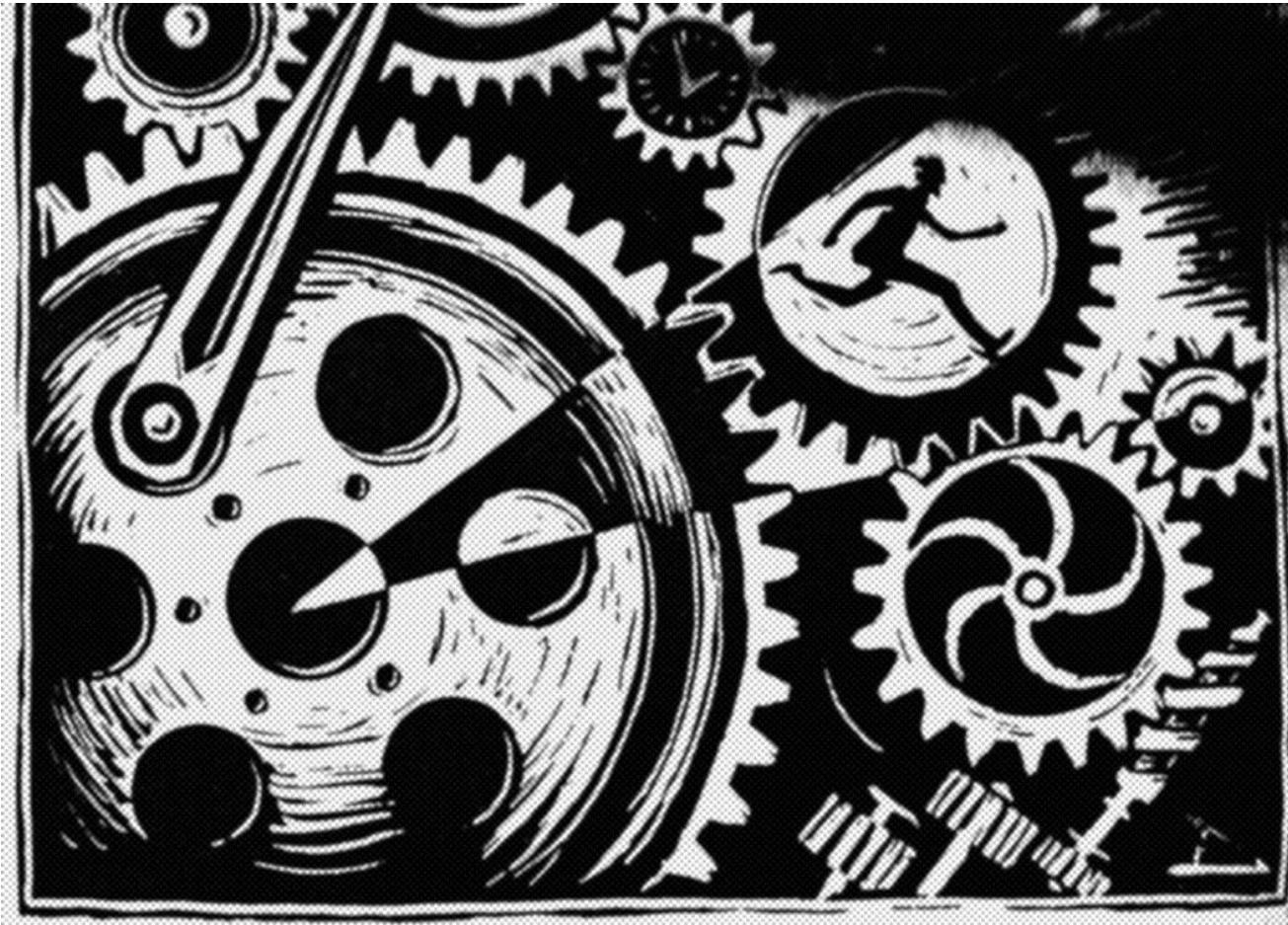
- June 2011-March 2012: Design of a DVB-S2 LDPC decoder for a Korean company (Private contract).
- Innovation: using “vertical scheduling” instead of “horizontal scheduling”.
- Size: 64 800 bits, rate  $\frac{1}{2}$  and  $\frac{2}{3}$  (proof of concept).
- Decoding throughput: 200 Mbit/s (information bit) with 36 decoding iterations on a Xilinx Virtex 5.

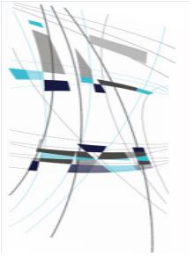
# Scenario of emulation.



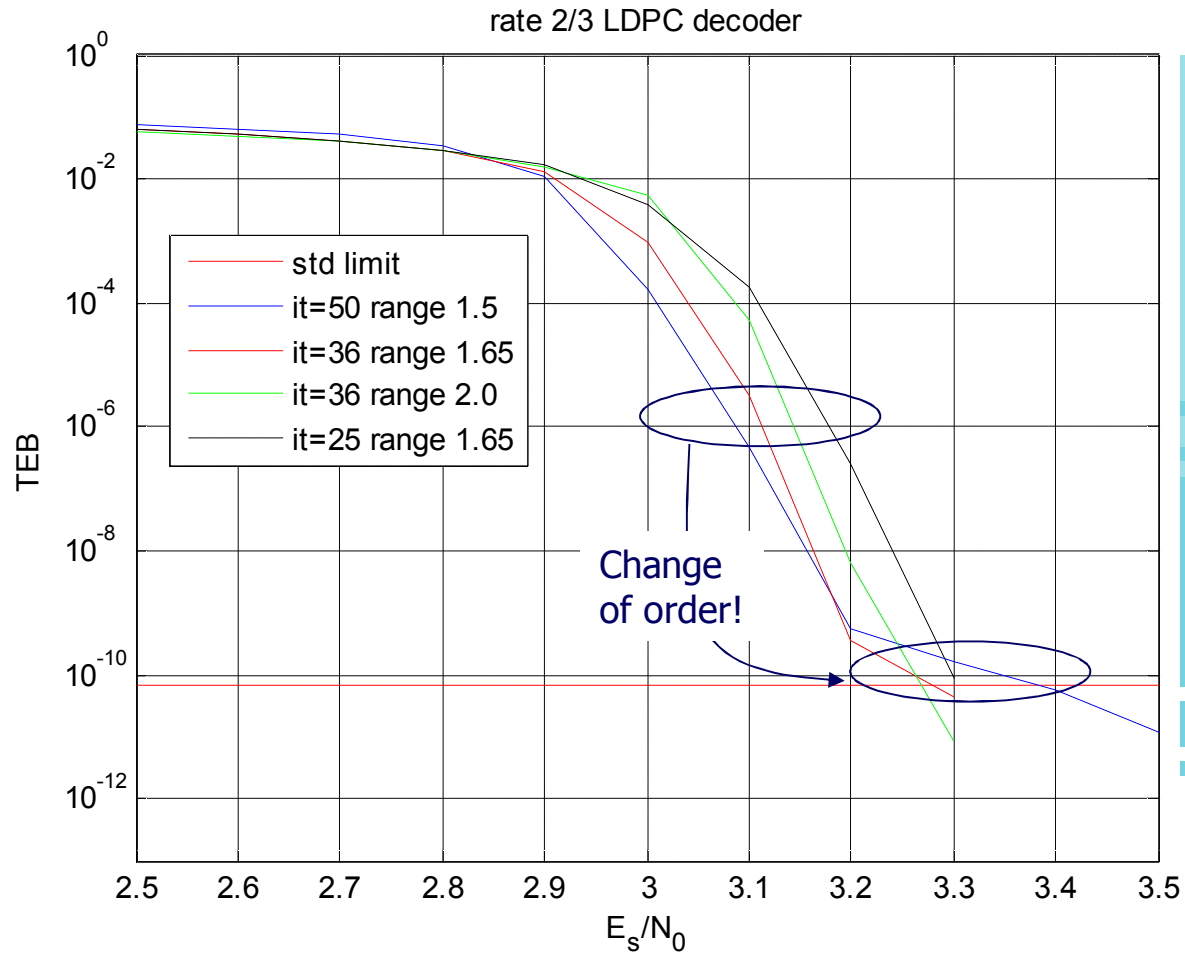


# Demonstration...





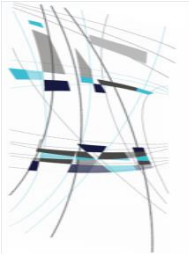
# After few days of simulations...



Range of BER that can be obtained by simulation in a reasonable time

Range of BER that can be obtained by hard emulation in a reasonable time





# Conclusion

- Methods to optimized error control code architecture using both simulation and emulation.
- So far, methods applied for:
  - ◇ NXP (CIFRE): LDPC DVB-S2 (schedul. horizontal).
  - ◇ Orange Labs (private contract): Code cortex
  - ◇ ETRI (Private contract): LDPC DVB-S2 (schedul. Vertical)
  - ◇ DaVinci (FP7): LDPC Non Binaire.