Abstract

Both the evolution of IC integration and digital communication protocols make it possible to think of the design of a "channel decoder" unique for a whole class of digital demodulation. Such a component, owing to its versatility, would allow to cope with the requirements of multiple applications. Thus, it could benefit from the reduction of the production cost linked to the mass production.

In order to define the requirements of such a receiver, channel decoding algorithms corresponding to several communication links (cable, satellite and terrestrial) for the "digital television" have been studied. This study leads naturally to a reduction of basic functions to filtering.

The resulting proposal is an heterogeneous parallel generic architecture for digital communication called "Parallel-Digital Communication Processor" (P-DCP), which basic component is an execution unit, called "Communication Co-Processor" (CCP), optimized for filtering operations. This parallel architecture is also based on a static interconnection network fully compliant with channel decoding constraints (low latency, high data rate, local communications) integrating a mechanism that copes with the dynamic communications required by the variable symbol rate.

This architecture allows to consider the genericity and the modularity of a multi-standard channel decoder. It should help accelerating the design of multiple purpose products. Then, the next step will be the conception of a "universal modem" used as an interface between any communication terminal (TV, PC, play station, telephone) and any communication link (cable, satellite, phone line, electrical line).