VLSI Architectures for Joint Source-Channel Trellis

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Conventionally, a digital communication system is composed of a source coder (reduction of the information to be transmitted) and a channel coder (protection against channel errors). This approach allows on the one hand to divide the transmission of information into two independent tasks, and on the other hand, to operate close to the theoretical limits for a given channel SNR. Nevertheless, this tandem system exhibits a high overall complexity and in addition, it suffers from a dramatic performance degradation when the channel conditions are poor. In this thesis, we focus on a joint source-channel trellis coding technique from both a theoretical and hardware standpoints. Our goal is to implement a simple and robust coding system for a large range of channel SNR and which could replace more efficiently the tandem system in certain applications.

The main goal of this joint source-channel trellis coding technique is to find a representation of the source sequence which minimizes the expectation of the distortion between the source sequence and the reproduction sequence decoded at the receiver end. This minimization is accomplished by a codebook design algorithm which takes into account the channel distribution during the generation of the reproduction codebook, and by the branch metric of the Viterbi algorithm employed during the quantization process.

In the first part of this work, we show that the type of computations required for the codebook design operation and the branch metrics of the Viterbi algorithm are quite similar. Upon proposing a simplification in the computations of the branch metric, a reconfigurable architecture is presented which allows to implement both the codebook design algorithm and the quantization process within the same architecture.

In the next stage of this work, complexity reductions were investigated by replacing the Viterbi algorithm with a suboptimum trellis search. We showed that the M algorithm, when used in the context of joint source-channel trellis coding, presented excellent complexity-performance trade offs. Then, we focused on the design of VLSI architectures for the M algorithm, and two new ideas which are potentially more advantageous than previously reported work are proposed. The first one profits from the trellis structure to reduce up to 50% the hardware complexity of the sorting networks required by this algorithm. The second idea consists in the adaptation of the trace-back technique employed in Viterbi decoders to the M algorithm with the use of pointer tables.

Finally, in the last part of this work, a joint source-channel coding technique is presented consisting in the joint optimization of the trellis quantizer described above and a convolutional code. The pairwise error probabilities required to perform the codebook design operation and the source quantization are derived from the generator polynomials of the convolutional code. Then, at the decoder end, we propose to decode the received channel sequence by means of the MAP algorithm. This algorithm provides us with the a posteriori probabilities of each trellis branch, or equivalently, with the probabilities of decoding a given codeword from the reproduction codebook. We called this a "soft" source decoding.