Optimization of Sign-Preserving Noise-Aided Min-Sum Decoders with Density Evolution or "forget the zero"

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Outline

1. Objectives
2. Introduction to Offset Min-Sum Based Decoders
3. Sign-Preserving Min-Sum (SP-MS) Decoders
4. Optimization of Sign Preserving Min-Sum Decoders
5. Implementation of SP-MS Decoders
6. Conclusions

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Objectives

Problem

Future optical applications will required Tbit/s efficient FEC decoder.

A priori of the study

Low precision decoders with 3 inputs bits.

Ambitions

New decoding algorithm called Sign-Preserving algorithm with

- Low performance degradation
- Very efficient hardware implementation

Example: IEEE 802.3 LDPC code (10 GbitEthernet) with 28 nm technology: 100 Gbit/s per mm^2.

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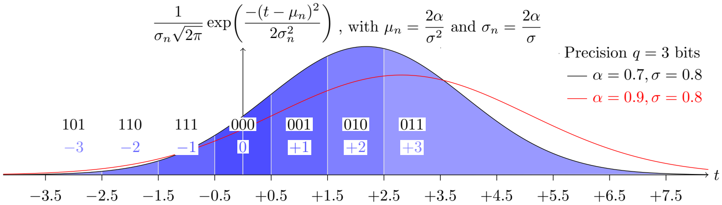
Classical OMS decoder: quantification of channel LLR

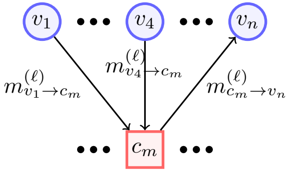
Quantified intrinsic information I_n is obtained from channel LLR y_n as $I_n = \mathcal{Q}(\alpha \times y_n)$, with $y_n \in \mathbb{R}$, α a scaling factor and $\mathcal{Q}$ a quantification rules from $\mathbb{R}$ to $\mathcal{A}_C = \{-3, -2, -1, 0, +1, +2, +3\}$ defined as $\mathcal{Q}(a) = \mathcal{S}_3(\lfloor a + 0.5 \rfloor)$, with $\mathcal{S}_3$ the saturation function toward [-3, 3].



Among the 8 levels of a 3 bits representation, only 7 are used.

- **Update rule at a CNU**

$$m^{(\ell)}_{c_m \to v_n} = \left(\prod_{v \in \mathcal{V}(c_m) \setminus \{v_n\}} \text{sign}\left(m^{(\ell)}_{v \to c_m} \right) \right) \times \max\left\{ \min_{v \in \mathcal{V}(c_m) \setminus \{v_n\}} \left| m^{(\ell)}_{v \to c_m} \right| - 1, 0 \right\}.$$

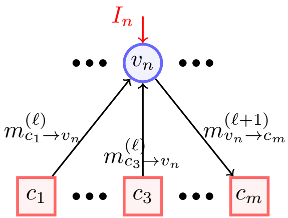


  - Note that for low precision $q = 3$ (same for $q = 4$), the offset applied in CNUs only gives us the possibility to use 5 values ($m^{(\ell)}_{c_m \to v_n} \in \{-2, -1, 0, +1, +2\}$) instead of the 7 values of $\mathcal{A}_C$.

- **Update rule at a VNU**

$$m_{v_n \to c_m}^{(\ell+1),U} = I_n + \sum_{c \in \mathcal{V}(v_n) \setminus \{c_m\}} m_{c \to v_n}^{(\ell)}.$$

exponent U indicates unsaturated message.



$$m_{v_n \to c_m}^{(\ell+1)} = \mathcal{S}_3 \left(m_{v_n \to c_m}^{(\ell+1),U} \right).$$

$$m_{v_n \to c_m}^{(\ell+1)} \in \{-3, -2, -1, 0, +1, +2, +3\}.$$

Low precision Offset Min-Sum Based Decoders

From the analysis of OMS-based decoders with $q = 3$

(i) the quantized LLRs $I_n \in \mathcal{A}_C = \{-3, -2, -1, 0, +1, +2, +3\}$,
(ii) v-to-c messages $m^{(\ell+1)}_{v_n \to c_m} \in \mathcal{A}_C = \{-3, -2, -1, 0, +1, +2, +3\}$, and
(iii) c-to-v messages $m^{(\ell)}_{c_m \to v_n} \in \mathcal{A}_C \backslash \{-3, +3\} = \{-2, -1, 0, +1, +2\}$.

The OMS-based decoders are suboptimal

It can be clearly noted that all combinations that can be obtained from $q = 3$ bits is not used.

How to use the 8 quantization levels for precision $q = 3$

We define a new decoder called Sign-Preserving decoder where:

- The quantization of LLRs has to be changed.
- CNU has to be changed.
- VNU has to be changed.

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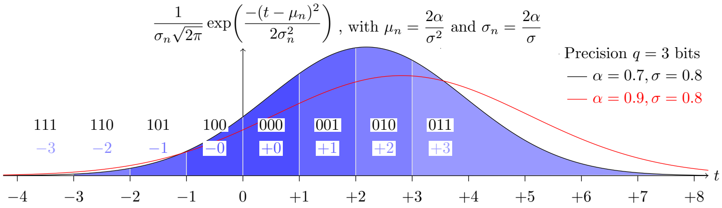
Quantization used for Sign-Preserving Min-Sum Decoders

- In order to use the 8 levels of $q = 3$ bits, we define the message alphabet as $\mathcal{A}_S = \{-3, -2, -1, -0, +0, +1, +2, +3\}$. Using the sign-and-magnitude representation we have $100_2 = -0$, $000_2 = +0$, etc.
- A new quantification process $\mathcal{Q}^*$ is used: $I_n = \mathcal{Q}^*(\alpha \times y_n) \in \mathcal{A}_S$ where $\mathcal{Q}^*(a) = (\text{sign}(a), \mathcal{S}_3(\lceil \alpha \times |a| \rceil - 1))$

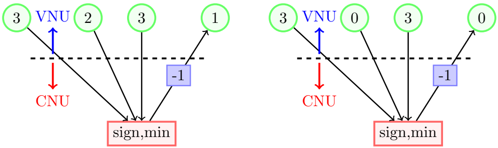


The *channel gain factor* α represents a degree of freedom in the decoder definition.

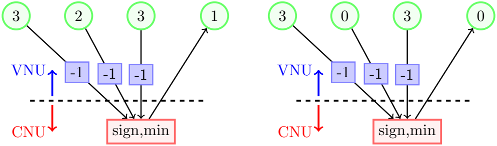
CNU of Sign-Preserving Min-Sum Decoders

The update rule at a CNU can be written in two equivalent ways.

Classical method: $\left|m^{(\ell)}_{c_m\to v_n}\right| = \max\left\{\min_{v\in\mathcal{V}(c_m)\setminus\{v_n\}}\left|m^{(\ell)}_{v\to c_m}\right| - 1, 0\right\}.$



Equivalent method: $\left|m^{(\ell)}_{c_m\to v_n}\right| = \min_{v\in\mathcal{V}(c_m)\setminus\{v_n\}}\left(\max\left(\left|m^{(\ell)}_{v\to c_m}\right| - 1, 0\right)\right).$



Therefore, we can move the offset from CNs to VNs.

VNU of Sign-Preserving Min-Sum Decoders

Moving the offset from CNs to VNs, the update rule at a VNU of OMS-based decoders can be rewritten as

$$m_{v_n \to c_m}^{(\ell+1),U} = I_n + \sum_{c \in \mathcal{V}(v_n) \setminus \{c_m\}} m_{c \to v_n}^{(\ell)}.$$

The offset is subtracted before saturation to allow -3 and 3 values in the variable to check message.

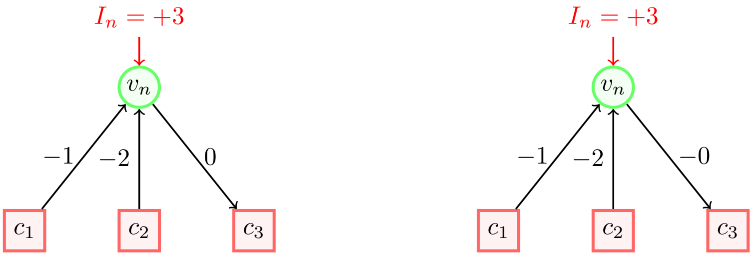
$$m_{v_n \to c_m}^{(\ell+1)} = \text{sign}\left(m_{v_n \to c_m}^{(\ell+1),U}\right) \times \mathcal{S}_3\left(\max\left(\left|m_{v_n \to c_m}^{(\ell+1),U}\right| - 1, 0\right)\right)$$

Problem of the update rule at VNUs

The v-to-c message $m_{v_n \to c_m}^{(\ell+1)}$ can be zero, zero does not have any information about the bit value, this means that the VNU can erase the bit value.

VNU of Sign-Preserving Min-Sum Decoders

Classical VNU: **Modified VNU:**



Idea to avoid the zero value.

- **Modified VNU:** we propose to use half the sum of the signs of the c-to-v messages and the sign of the quantized LLR
Example: $a = (+\mathbf{3}-\mathbf{1}-\mathbf{2}) + (+\mathbf{1}-\mathbf{1}-\mathbf{1})/2 = -\mathbf{0.5}$, hence $m^{(\ell),U}_{v_n \to c_3} = (\text{sign}(a), \lfloor |a| \rfloor) = -\mathbf{0}$ and $m^{(\ell)}_{v_n \to c_3} = -\mathbf{0}$.

We define the Sign-Preserving Min-Sum decoders as decoders that always preserve the sign of the messages.

Let us denote by $\mu^{(\ell)}_{v_n \to c_m}$ the *sign-preserving factor* of the message $m^{(\ell+1)}_{v_n \to c_m}$, defined as

$$\mu^{(\ell)}_{v_n \to c_m} = \xi \times \text{sign}(I_n) + \sum_{c \in \mathcal{V}(v_n) \setminus \{c_m\}} \text{sign}\left(m^{(\ell)}_{c \to v_n}\right),$$

where $\xi = \begin{cases} 0, & d_v = 2, \\ 1, & d_v \in \{3, 5, 7, ...\}, \\ 2, & d_v \in \{4, 6, 8, ...\}. \end{cases}$

By construction $\mu^{(\ell)}_{v_n \to c_m}$ take its value between $\{-1, 1\}$ for $d_v = 2$, $\{-d_v, -d_v + 2, \ldots, -1, 1, \ldots, d_v\}$ for d_v odd and $\{-d_v - 1, -d_v + 1, \ldots, -1, 1, \ldots, d_v + 1\}$ for d_v even.

Update rules for SP-MS Decoders

- Let us redefined $m_{v_n \to c_m}^{(\ell+1),U}$ as

$$m_{v_n \to c_m}^{(\ell+1),U} = \frac{\mu_{v_n \to c_m}^{(\ell)}}{2} + I_n + \sum_{c \in \mathcal{V}(v_n) \setminus \{c_m\}} m_{c \to v_n}^{(\ell)}$$

- $m_{v_n \to c_m}^{(\ell+1),U}$ takes its value in the set $\mathcal{A}_U = \{\ldots, -1.5, -0.5, +0.5, +1.5, \ldots\}$.
- and we obtain a message $m_{v_n \to c_m}^{(\ell+1)}$ that has always a defined sign as

$$m_{v_n \to c_m}^{(\ell+1)} = \left(\text{sign}\left(m_{v_n \to c_m}^{(\ell+1),U}\right), \mathcal{S}_3\left(\max\left(\left\lfloor \left| m_{v_n \to c_m}^{(\ell+1),U} \right| \right\rfloor - 1, 0\right)\right)\right).$$

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Optimization of Sign-Preserving Min-Sum Decoders

In order to optimize the SP-MS decoders, we use the optimization method proposed in [1], *i.e.*, we introduce a certain level of randomness in the optimization process. The optimization process is given by

$$\tilde{m}_{v_n \to c_m}^{(\ell+1)} = \Upsilon\left(m_{v_n \to c_m}^{(\ell+1),U}\right),$$

Where Υ is a noise model that also performs the saturation function. After optimization we can obtain two kinds of decoders:

- A decoder that keeps some randomness named Sign-Preserving Noise-Aided Min-Sum (SP-NA-MS) decoder.
- Or a deterministic decoder named in general Sign-Preserving Min-Sum (SP-MS) decoder.

A Probabilistic Error Model

The noise models need to be memoryless and have to satisfy the symmetry condition $\Pr(\Upsilon(\beta_1) = \beta_2) = \Pr(\Upsilon(-\beta_1) = -\beta_2), \quad \forall \beta_1, \beta_2$.

- $\Upsilon : \mathcal{A}_U \to \tilde{\mathcal{A}}_S$, where $\tilde{\mathcal{A}}_S = \mathcal{A}_S$, denotes the function which transforms $m_u = m_{v_n \to c_m}^{(\ell+1),U} \in \mathcal{A}_U$ into $\tilde{m} = \tilde{m}_{v_n \to c_m}^{(\ell+1)} \in \tilde{\mathcal{A}}_S$. Υ is defined by the conditional PDF (CPDF) $\Pr(\Upsilon(m_u) = \tilde{m})$.

$m_u =$	$+0.5$	$+1.5$	$+2.5$	$+3.5$	$> +3.5$
$\tilde{m} = +3$	0	0	0	$1 - \varphi_s$	1
$\tilde{m} = +2$	0	0	$1 - \varphi_a$	φ_s	0
$\tilde{m} = +1$	0	$1 - \varphi_0$	φ_a	0	0
$\tilde{m} = +0$	1	φ_0	0	0	0

Table: CPDF of Υ.

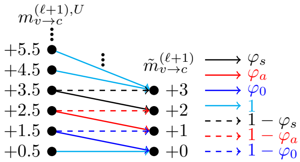
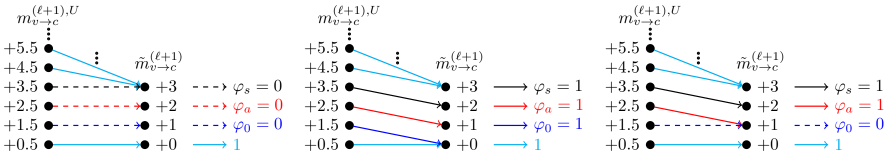


Figure: Noise model.

$\boldsymbol{\varphi} = (\alpha, \varphi_s, \varphi_a, \varphi_0)$ will be optimized with the noisy DE tool.

Example of SP-MS decoders for regular LDPC codes



(a) SP-MS. (b) SP-OMS. (c) Optimized SP-MS.

		MS Decoder	OMS decoders	SP-NA-MS decoders	Optimized SP-MS		
(d_v, d_c)	q	δ_{db}	δ_{db}	$\tilde{\delta}_{db}$	δ_{db}	DE gain	SNR gain
$(3,6)$	3	**1.7888**	2.2039	**1.4994**	1.5096	**0.2894**	**0.27**
	4	1.6437	**1.3481**	**1.2688**	**1.2688**	**0.0793**	**0.06**
$(4,8)$	3	2.7360	**2.3219**	**1.9820**	1.9824	**0.3399**	**0.32**
	4	2.5389	**1.7509**	**1.7306**	**1.7306**	**0.0203**	**0.0**
$(5,10)$	3	3.4117	**2.7079**	**2.4908**	**2.4908**	**0.2177**	**0.21**
	4	3.1772	**2.2306**	**2.2196**	**2.2196**	**0.0110**	**0.007**
$(6,32)$	3	4.0812	**3.5928**	**3.3963**	**3.3963**	**0.1965**	**0.19**
	4	3.8154	**3.1685**	**3.1787**	**3.1787**	**-0.0102**	**0.0**

SNR gains in the waterfall correspond to what was predicted with DE.

FER performance for the (3,6)-regular LDPC code

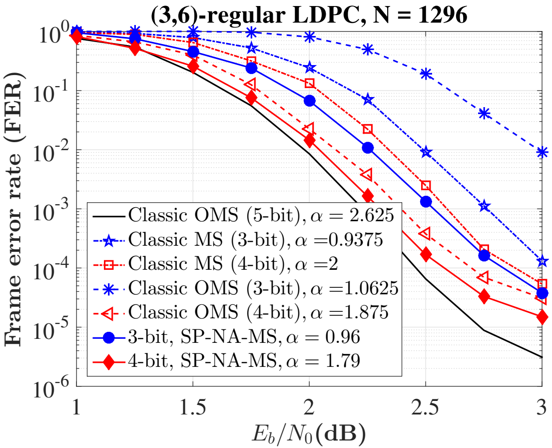


Figure: For $q = 3$, DE gain $=$ 0.2894 and SNR gain $=$ 0.27. For $q = 4$, DE gain $=$ 0.0793 and SNR gain $=$ 0.06.

SP-MS decoders for Irregular LDPC codes

Here we present the DE thresholds results and the FER performance for the WIMAX rate 1/2 LDPC code.

Irregular LDPC code, BI-AWGN channel					
		MS Decoder		OMS decoders	
R	q	α^*	δ_{db}	α^*	δ_{db}
1/2	3	0.44	**1.8310**	0.40	5.2283
	4	1.07	**1.3941**	0.80	2.8140

Irregular LDPC code, BI-AWGN channel					
		SP-NA-MS		Optimized SP-MS	
R	q	α^*	$\tilde{\delta}_{db}$	α^*	δ_{db}
1/2	3	0.65	**1.3997**	0.65	1.4003
	4	1.24	**0.9547**	1.24	0.9582

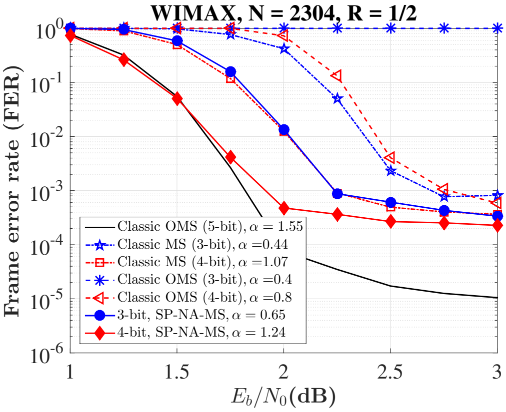


Figure: For $q = 3$, DE gain $= 0.4313$ and SNR gain $= 0.40$. For $q = 4$, DE gain $= 0.4394$ and SNR gain $= 0.40$.

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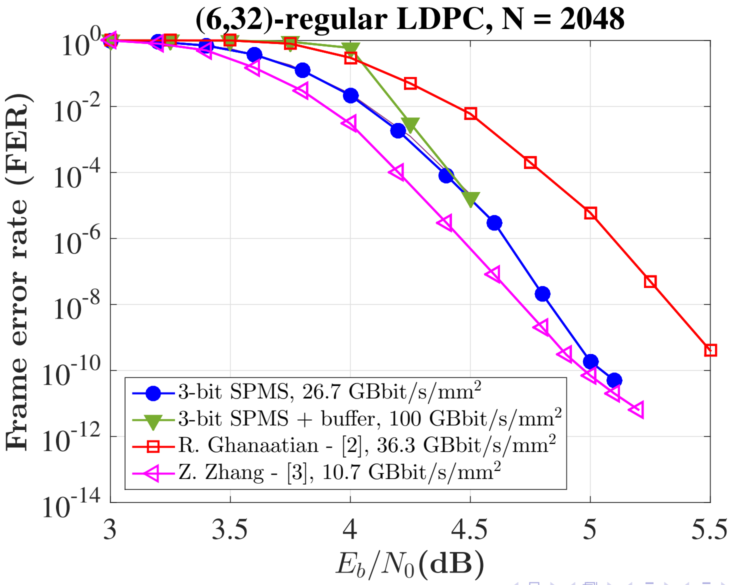
Synthesis results for regular LDPC Codes

IEEE 802.3 LDPC code: Rate 0.8143 $(2048, 1723)$ with regular $(6, 32)$ degree distribution.

	This work	Ghanaatian,2018,[2]	Zhang,2010,[3]
Technology	28nm FDSOI	28nm FDSOI	65nm CMOS
Decoder	SP-MS	finite-alphabet	OMS
Quantization	3 bits	3 bits	4 bits
Iterations	9+6	5	8+6
Architecture	full-parallel	unrolled full-parallel	partial-parallel
E_b/N_0 @ FER= 10^{-10}	5.03 dB	5.51 dB	4.98 dB
Frequency	500 MHz†	862 MHz	700 $\xrightarrow{28nm}$ 1000 MHz
Core area	2.56 mm^{2†}	16.2 mm^2	5.05 $\xrightarrow{28nm}$ 1.77 mm^2
Throughput	68.3 Gbit/s†	588 Gbit/s	13.3 $\xrightarrow{28nm}$ 19 Gbit/s
Hardware efficiency	26.7 Gbit/s/mm^{2†}	36.3 Gbit/s/mm^2	2.63 $\xrightarrow{28nm}$ 10.7 Gbit/s/mm^2
Throughput (4.5 dB)	256 Gbit/s/mm^{2†}	588 Gbit/s/mm^2	33.3 $\xrightarrow{28nm}$ 48.2 Gbit/s/mm^2
Hardware efficiency (4.5 dB)	100 Gbit/s/mm^{2†}	36.3 Gbit/s/mm^2	6.59 $\xrightarrow{28nm}$ 26.91 Gbit/s/mm^2

† Preliminary results.

Emulation on FPGA for the IEEE 802.3 ETHERNET code



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Conclusions

Proposition of the Sign-Preserving Min-Sum algorithm for low bit precision iterative decoder.

Density evolution techniques to optimize the application of offset value at variable node level. Performance simulation for finite regular/irregular code consistent with DE analysis.

Emulation results on FPGA + ASIC synthesis result for the IEEE 802.3 ETHERNET code. Tera bit/s decoding throughput is feasible in an ASIC.

Future work: extend the method for others type of low precision decoders (Turbo-Code, Polar Code,...).

Thank you for listening!

Questions?

References I

[1] F. Cochachin, D. Declercq, E. Boutillon, and L. Kessal, "Density Evolution Thresholds for Noise-Against-Noise Min-Sum Decoders", *2017 IEEE 28th Annual International Symposium on Personal, Indoor, and Mobile Radio Communications (PIMRC)*, pp. 1–7, Oct 2017. DOI: 10.1109/PIMRC.2017.8292326.

[2] R. Ghanaatian, A. Balatsoukas-Stimming, T. C. Müller, M. Meidlinger, G. Matz, A. Teman, and A. Burg, "A 588-gb/s ldpc decoder based on finite-alphabet message passing", *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, vol. 26, no. 2, pp. 329–340, Feb 2018, ISSN: 1063-8210. DOI: 10.1109/TVLSI.2017.2766925.

[3] Z. Zhang, V. Anantharam, M. J. Wainwright, and B. Nikolic, "An efficient 10gbase-t ethernet ldpc decoder design with low error floors", *IEEE Journal of Solid-State Circuits*, vol. 45, no. 4, pp. 843–855, April 2010, ISSN: 0018-9200. DOI: 10.1109/JSSC.2010.2042255.