Recent Advances on Stochastic and Noise Enhanced Methods in Error Correction Decoders

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***Abstract*—This paper offers a review of recent developments in non-deterministic error correction decoding methods, which can be described in two broad classes. The first class uses stochastic computation to emulate the arithmetic operations of conventional decoding algorithms. The second class achieves noise enhancement by randomly perturbing the calculations of a standard decoder. Stochastic decoders inherit analysis techniques from the conventional algorithms they emulate, but the noise-enhanced algorithms are newer, more difficult to explain, and not yet fully understood. We describe a Markov chain analysis technique to both explain and optimize noise enhancement in these algorithms. Circuit implementation is also discussed, including both conventional hardware architectures and circuits based on memristor threshold logic, where memristor non-determinism can be exploited for noise enhancement.**

I. Introduction

Non-deterministic algorithms are well known in a variety of fields (optimization, imaging, neuromorphic computing, etc), in which the performance or efficiency is enhanced beyond what could be obtained by a deterministic method. For many years, there has been a corresponding interest in reliable or fault-tolerant computing with non-deterministic physical components. In this paper we survey a family of non-deterministic error correction algorithms and circuit implementations that merge these topics, providing a useful framework for noise enhancement at the physical layer of data communication, memory and storage. Most of the recent advances in this area focus on Low Density Parity Check (LDPC) codes, a well known class of error correction algorithms that are now included in numerous data communication standards. The survey will therefore be limited to the domain of LDPC codes, though the concepts are by no means restricted to that class of codes.

LDPC codes are used to encode data by inserting redundant parity bits in anticipation of corruption due to noisy communication channels or faulty memory cells. Error correction is usually done using Bayesian Belief Propagation (BP) or related algorithms. BP-based algorithms perform exceptionally well in that they achieve very low error rates after decoding retrieved data. An alternative class of Bit-Flipping (BF) algorithms is also widely studied. BF decoders are much simpler to implement in hardware, but achieve comparatively poor error rates. During the past two decades, a great deal of research has been invested into designing algorithms that optimize the tradeoff between BP's excellent performance and BF's simplicity.

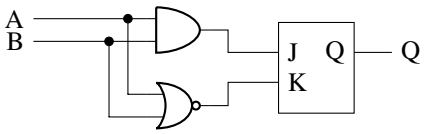


Fig. 1: Stochastic variable node implementation based on a Muller C-element with J/K flip-flop.

A. Review of stochastic decoding algorithms

LPDC decoders belong to a class of message-passing algorithms defined on factor graphs. A message passing decoder computes local probability or likelihood metrics at each node. Local calculations are iterated until all parity-check constraints are satisfied, indicating global convergence.

A typical BP-based decoder must perform a number of integer additions, lookup table operations, or comparisons to obtain a metric for every edge in the graph. In order to reduce the hardware cost of these decoders, beginning in 2003 researchers considered stochastic computing methods to emulate the required arithmetic [1]. The basic concept is to compute probability metrics by filtering pseudorandom bit sequences that model a Bernoulli process. A probability value is directly encoded in the frequency of 1's appearing in the sequence. The hardware is often simpler than BP-based decoders: adders are replaced by Muller C-element gates (similar in function to J/K flip-flops). An example C-element implementation is shown in Fig. 1. In the figure, the processor receives two input Bernoulli streams, A and B, with statistics p_A and p_B, respectively. It is well known that the output is a sequence with statistic

$$p_Q = \frac{p_A p_B}{p_A p_B + (1-p_A)(1-p_B)}$$

which corresponds to the BP symbol node operation.

For an acyclic graph, a stochastic decoder has performance equivalent to BP. Most code graphs are cyclic, and in this case the stochastic algorithm becomes trapped in deterministic

patterns, resulting in uncorrectable error patterns along the cyclic subgraphs. To resolve this problem, the variable node implementation (Fig. 2) is modified to have non-deterministic behavior [2]. The best performing modification is the family of "edge memory" methods, which restore performance close to BP [3]. An edge memory is a module that samples the statistics of an input bit stream, and emits a separate, independent stream with the same statistics. If an edge memory is inserted in every cycle within the decoder, then deterministic loops are eliminated while preserving the BP-based probability calculations.

B. Noise enhanced decoders

Arguably the first observation of non-deterministic enhancement was in 2001, in the context of analog decoders where device mismatch was observed to enhance performance in some cases [4]. This phenomenon was explained by the sub-optimality of BP on cyclic code graphs, which opened a possibility for accidental improvement in randomly altered designs. A more systematic approach to noise enhancement appeared with probabilistic bit flipping (PBF) in 2005, where Gallager-style bit-flipping algorithm was modified to flip bits only with probability p (i.e. the algorithm's normal bit flips are suppressed with probability $1-p$) [5]. In 2009, noise enhancement was observed for stochastic decoders implemented with a mixture of permanent defects and transient errors [6], where noise-induced upsets were found beneficial for compensating permanent faults.

In 2012, dithered belief propagation was described, marking the first explicit construction of a noise enhanced BP decoder where decoding operations are deliberately perturbed by artificial noise [7]. This was followed soon after by four developments in 2014. First, noise enhancement was observed for the BP-based Min-Sun (MS) algorithm on the binary symmetric channel (BSC) [8]. In the same year, Noisy Gradient Descent Bit Flipping (NGDBF) was described for the Gaussian channel [9] and the related Probabilistic Gradient Descent Bit Flipping (PGDBF) algorithm for the BSC [10]. These works led to a number of algorithm and hardware improvements for NGDBF [11]–[13] and PGDBF [14]–[17], along with potential specialized applications in solid-state storage [18]. A related approach, known as the Improved Differential Binary (IDB) decoder, was also proposed in 2014 [19]. The IDB decoder uses a combination of feedback (similar to the stochastic TFM) and perturbed threshold operations.

The GDBF algorithm is based on sum-and-threshold operations, as shown in Fig. 2. First, a hard decision syndrome vector is computed by the parity-check nodes. Then, for each variable node, an "energy function" is computed (also called a "reliability" or "flipping" function) by the expression

$$E_k^{(\text{GDBF})} = x_k y_k + \sum_{j \in \mathcal{M}_k} s_j, \tag{1}$$

where y_k is the channel information, $x_k \in \{+1, -1\}$ is the bipolar hypothesis decision, $\mathcal{M}_k$ is the parity-check

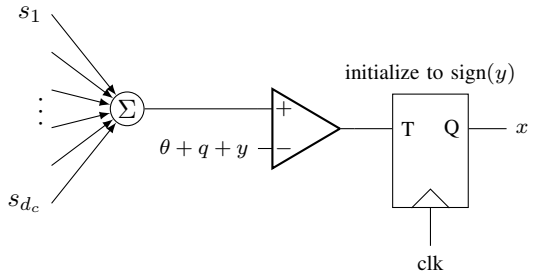


Fig. 2: Typical variable node implementation for the NGDBF algorithm based on a toggle flip-flop. Inputs are channel information y, threshold θ, random perturbation q, and adjacent parity-check messages s_j.

neighborhood of the k^{th} variable node, and the s_j are bipolar syndrome values (parity is satisfied when $s_j = +1$ and violated when $s_j = -1$). In each iteration, the decision x_k is flipped if $E_k < \theta$, where θ is a threshold that may vary from iteration to iteration or, in some algorithms, from node to node.

In the NGDBF algorithm, the threshold operation is perturbed by injected noise q:

$$E_k^{(\text{NGDBF})} = x_k y_k + \sum_{j \in \mathcal{M}_k} s_j + q, \tag{2}$$

In the PGDBF algorithm, the sum-and-threshold operation is carried out using the GDBF rule (1), and if $E_k < \theta$ then the bit is flipped only with probability p_{flip}. In the NGDBF and PGDBF algorithms, some kind of random number generator (RNG) is needed to generate the non-deterministic behavior. For NGDBF, Gaussian perturbations have generally been used, but other distributions have also been used with a small performance penalty [9]. There are now numerous variations on the NGDBF and PGDBF algorithms, which differ mainly in the method and scheduling of how θ is determined.

Besides bit-flipping and BP-based decoders, other types of noise-enhanced decoders have been reported, such as a recent stochastic BCH decoder [20] and a stochastic Chase algorithm [21]. These are often described as stochastic decoders, however they do not utilize the hardware techniques traditionally labeled as "stochastic computing" and are arguably more similar to noise-enhanced decoders than to the BP-based stochastic decoders described in Sec. I-A, since they perform a discrete codeword search aided by non-determinism. Research on noisy BP-based decoders has also continued to advance, as with the recent Noise-Against-Noise Decoder (NAND) algorithm [22].

II. Theory

The development of noise-enhanced decoders was experimentally driven, and significant performance enhancing effects were discovered and optimized empirically prior to developing a sound theoretical footing. The empirical approach nevertheless realized a high degree of performance gain. One example is shown in Fig. 3, which compares performance of stochastic and NGDBF algorithms with ideal BP decoding on the AWGN

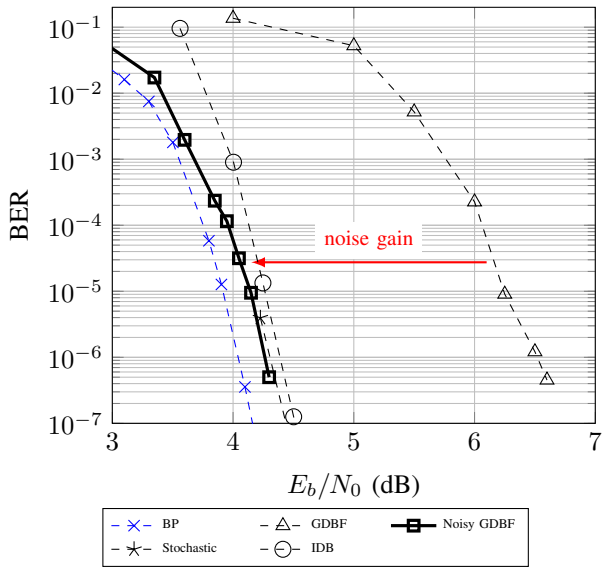


Fig. 3: Example of noise-enhanced performance for stochastic, IDB and NGDBF algorithms, applied to the IEEE 802.3an 10GBase-T standard. NGDBF allows a maximum of 600 iterations to decode a frame.

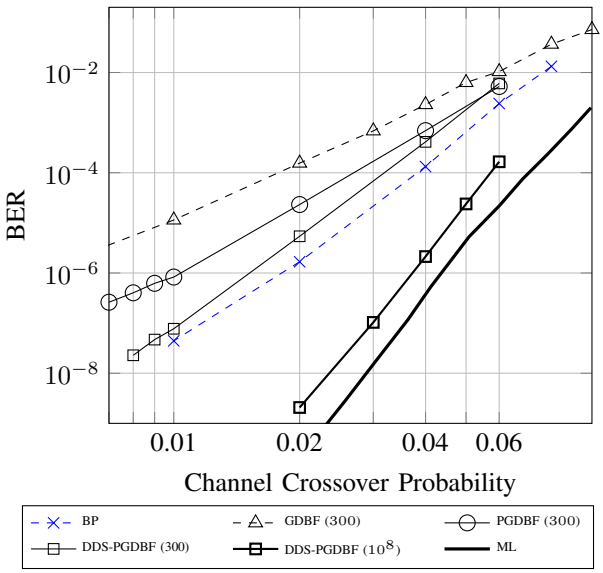


Fig. 4: Example of ML-approaching performance for the PGDBF algorithm on the Tanner code with $N = 155$. For each algorihtm, the maximum allowed iterations per frame are indicated in parentheses.

channel. Compared to noiseless GDBF, the leap in performance due to solely to noise is particularly striking. A second example is shown in Fig. 4, which shows performance of a "decoder-dynamic shift" (DDS) PGDBF algorithm [23] approaching maximum-likelihood performance on the BSC when a large iteration limit is allowed. The noise gains depicted in Figures 3 and 4 were discovered essentially by accident, and theoretical explanations came later. To date, the most productive explanation is that noise tends to disrupt trapping sets in the GDBF decoder. Trapping set analysis aids in parametric optimization for noisy decoders, but does not support ensemble optimizations like the ones obtained with density evolution for BP-based decoders.

LDPC codes are represented by compact graphs with many cycles, which break the formal correctness of BP and related algorithms. Certain error patterns can be difficult or impossible to correct on cyclic subgraphs known as trapping sets. In the case of BP-based algorithms, trapping sets are well known as the cause of error floors. In the domain of bit-flipping algorithms, trapping sets have proven useful for understanding and optimizing noise enhancement effects.

A Markov process approach to trapping sets was previously described [23], and is here illustrated by a simple example. We consider a trapping set involving m variable nodes. Then there are 2^m possible binary states for the variable nodes involved in the trapping set. Only one of these states is correct, and without loss of generality we assume it is state 0. Since the decoding algorithm is non-deterministic, in each iteration it may undergo a transition from its present state s_i to any other allowed state s_j with probability p_{ij}, hence the decoding iterations constitute a homogeneous Markov chain characterized by a square transition matrix Γ of dimension 2^m with entries p_{ij}.

For an initial erroneous state $\vec{s}_0$, the probability that the error is corrected after L iterations is the zeroth element of $\vec{s}_0\Gamma^L$. Since Γ and s_0 depend on the received channel information, we use a Markov Chain Monte Carlo procedure to evaluate the trapping set's contribution to the error probability over many frames. This procedure reveals that noise is essential for BF algorithms to correct trapping set errors. Furthermore, since Γ is dependent on various algorithms parameters (e.g. the noise statistics and distribution, weighting or clipping of channel samples, etc), these parameters can be adjusted and optimized at design time [24].

III. Implementation

A. Conventional ASIC and FPGA architectures

ASIC implementations of stochastic and noise enhanced BF decoders usually are fully parallel architectures that precisely map the code's factor graph topology. The circuit implementations have few degrees of freedom for the variable and check nodes, hence most design effort tends to focus on generating and distributing random numbers or on the design of efficient edge memories. Recent stochastic decoders proved competitive with BP-based decoders in both performance and silicon area [25]. More recent BF implementations require $2\times$ to $3\times$ less area than stochastic decoders, with similar or better decoding performance. The area reduction is explained by the data flow architectures shown in Fig. 5. In every iteration, stochastic decoders must compute two messages for every edge in the factor graph, whereas the BF decoders need only compute one message per node.

The normalized power consumption of BF decoders, reported in Joules per bit, is the lowest among decoders implemented in comparable technology. Due to their non-deterministic convergence, stochastic and noisy BF decoders cannot guarantee the same latency for all frames, and may require buffering frames to accommodate occasional delays. The average throughput is nevertheless high enough for major data communication standards, such as IEEE 802.3an 10GBase-T [11], [25].

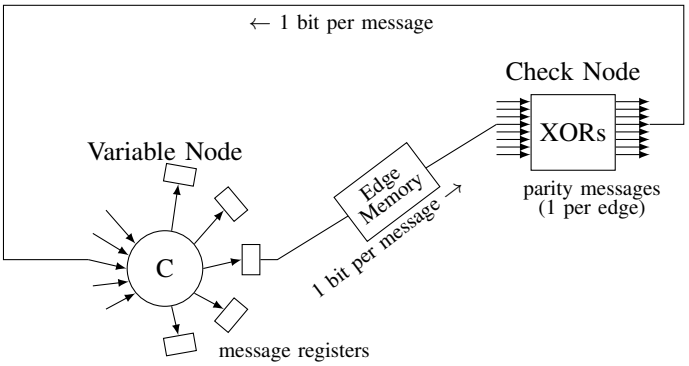
Non-deterministic BF decoders have been reported to perform well with a variety of non-ideal random number sources. Where the earliest designs typically employed linear feedback shift registers (LFSRs) to produce random numbers, it would be prohibitive to include an LFSR in every variable node. This motivated random sample reuse, where a large shift register is used to distribute samples from a single RNG [9]. Simpler approaches use no RNG at all, as random samples can be pre-generated as initialization values for a circular shift register [11]. Another LFSR-free approach uses an "intrinsic valued random generator" to extract random numbers from switching activity within the decoder [26].

For quasi-cyclic LDPC (QC-LDPC) codes, the recently described Variable Node Shift Architecture (VNSA) implements PGDBF without requiring any RNG [17]. In the VNSA, a unique pre-generated noise sample is hard-coded into each variable node. The code's structure permits cyclically shifting the variable node states after each iteration. With each iteration, the variable nodes' logical positions are shifted to new physical locations, where they obtain an updated noise sample from the local hardware instantiation. The VNSA decoder has hardware area almost as low as GDBF, making it one of the most area efficient decoder architectures.

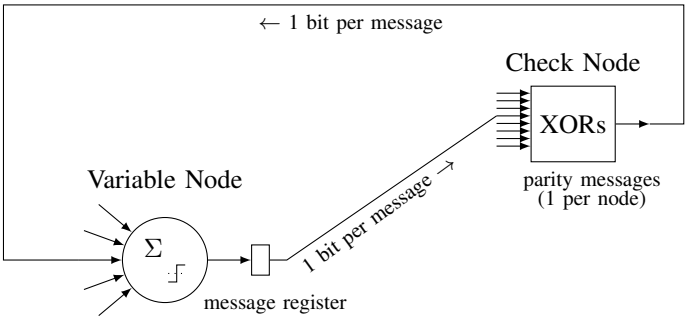
B. Unconventional emerging devices: memristors

In the development of stochastic and noise-enhanced decoders, two central points emerged: first, deterministic logic is fatal for stochastic decoders with cycles; second, non-determinism is essential for performance gain in noise enhanced decoders. In hardware implementation, non-determinism is usually provided using RNG circuits that incur substantial overhead in area and power. There is now an interest in exploiting nano-scale "native non-determinism" as a computational resource to mitigate the hardware cost of RNGs.

Recent research points to resistance-switching devices, commonly identified as a subclass of memristors, as having non-deterministic switching statistics that can be modeled with some precision, and can be adjusted by manipulating pulse timing or amplitude in memristive logic circuits [27]. A memristor of this type can be induced to switch between high-resistance and low-resistance states by applying forward and reverse voltages (respectively) in excess of the device's threshold voltage. When a lesser sub-threshold voltage is applied, the device's switching is a stochastic process. This phenomenon already attracted interest from the neuromorphic circuits community, where



(a) Single-bit message passing decoder.



(b) True bit-flipping decoder.

Fig. 5: Comparison of iterative data flow in stochastic vs BF architectures.

stochastic switching provides a model for neural networks based on spike timing dependent plasticity (STDP) [27], [28]. Memristor circuits were previously considered for LDPC decoders [29], and for stochastic computation [30].

A possible memristor-based randomness source is shown in Fig. 6. The memristor is initialized in a high-resistance state by applying a reverse pulse V_{rst} which exceeds the memristor's switching threshold. A train of sub-threshold pulses are then applied at V_p. A sub-threshold pulse can cause the memristor to switch to a low-resistance state with probabiilty p_{sw}. The switching statistics are a function of the pulse amplitude and width [27]. The memristor's resistance state is detected by monitoring the voltage in the resistor divider circuit formed by R. Each time the memristor switches to a low-resistance state, a reset cycle is required to restore the memristor to its high-resistance condition. The digital output Q is a true random Bernoulli sequence. Memristor-based random generators therefore have the potential to produce random perturbations with superior statistical features (i.e. true random instead of pseudo-random sequences), with less circuit area than traditional RNGs.

IV. Conclusion

This paper gave an abbreviated review of recent progress in stochastic and noise-enhanced decoding, emphasizing advances during the past five years. Progress in this topic appears to be accelerating and there are now applications for commercial

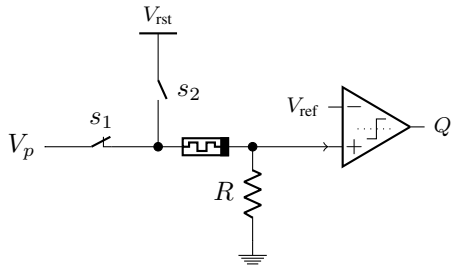


Fig. 6: A memristor-based randomness source.

standards. Better theoretical tools are still needed to understand convergence behavior and optimize throughput, to establish performance bounds, and to determine optimal code constructions for use with these algorithms. With the introduction of memristor circuits, new territory is now opened for continued research and discovery bridging the physical and algorithmic foundations of communication and memory.

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