The Best, the Requested, and the Default Elementary Check Node for EMS NB-LDPC Decoder

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General Introduction

- Channel Coding is an essential block in the digital communication chain.
- It allows reliable delivery of data over unreliable channels.
- Low-Density Parity Check (LDPC) codes are one of powerful Error-Correction Codes that allow approaching the theoretical capacity of the channel (Shannon's capacity).

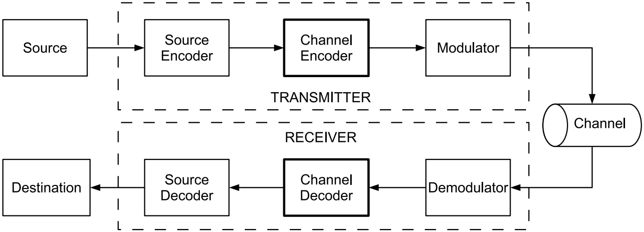

Figure 1: Digital Communication Chain.

Non-Binary LDPC Codes and Decoders

- NB-LDPC codes are extension of binary LDPC codes with $GF(q = 2^p)$ where $p > 1$ [1].
- Preserves decoding performance at short-frame transmission and high-order modulation [2].
- Standardized in Chinese Navigation Satellite System (BeiDou) and adopted in Consultative Committee for Space Data Systems (CCSDS).
- Information block of size K symbols on GF(q) is encoded to a code block of size N symbols by adding M redundant symbols.
- Decoder consists of M Check Nodes (CNs) and N Variable Nodes (VNs).
- Each CN C_i is connected to d_c VNs, denoted as check degree of connectivity.
- Each VN V_j is connected to d_v CNs, denoted as variable degree of connectivity.

Non-Binary LDPC Codes and Decoders

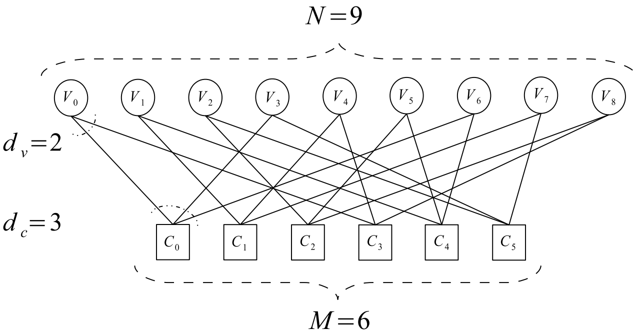

Figure 2: Tanner Graph of NB-LDPC Decoder

Non-Binary LDPC Codes and Decoders

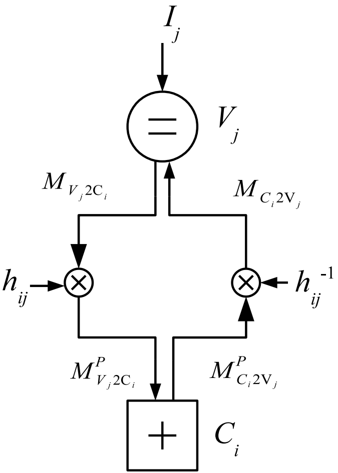

Figure 3: An Edge Connecting VN V_j to CN C_i.

Forward-Backward Extended Min-Sum Algorithm for NB-LDPC

- Complexity of NB-LDPC decoder is dominated in its CNs.
- In Min-Sum algorithm [3], CN updates d_c check-to-variable messages by processing $d_c \times q$ messages from connected VNs.
- Extended Min-Sum (EMS) is proposed in [4] to reduce complexity of CNs.
- How?
  - By truncating size of messages from q down to n_m.
  - Reducing check node operations from q^2 down to n_m^2.

Forward-Backward Extended Min-Sum Algorithm for NB-LDPC

- Forward-Backward approach [5] implements EMS algorithm by decomposing CN into 3 layers each of $d_c - 2$ Elementary Check Nodes (ECNs).

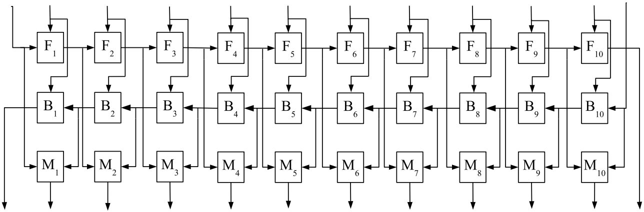

Figure 4: CN Decomposition in Forward-Backward Approach for $d_c = 12$

- ECN generates n_m candidates (GF and LLR couples) sorted in descending order of their reliability.

NB-LDPC Algorithms in Real-Life

Figure 5: Min-Sum in Real Life Scenario

NB-LDPC Algorithms in Real-Life

Figure 6: Extended Min-Sum in Real Life Scenario

NB-LDPC Algorithms in Real-Life

Figure 7: The Best, Requested, and Default in Real Life Scenario

The Best, Requested, and Default Algorithm

- The Best, Requested, and Default (BRD) algorithm [6] is generic NB-LDPC decoding algorithm.
- Allows VNs to request specific symbols from CNs.
- Requested symbols preserve decoding performance with shorter message sizes.

The Best, Requested, and Default Algorithm

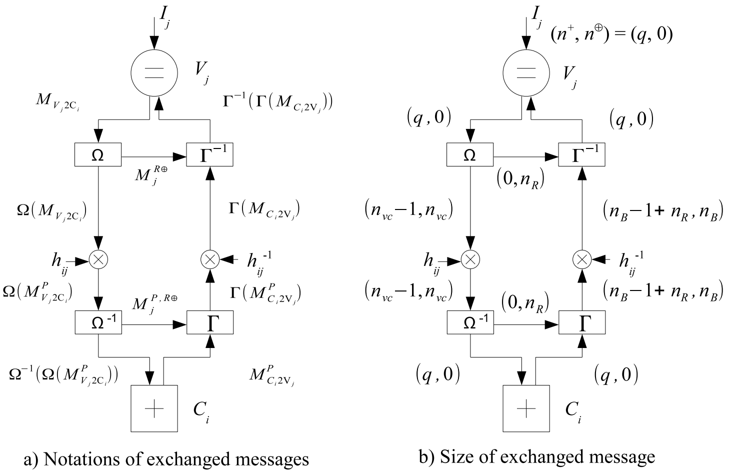

Figure 8: An Edge of BRD-based Nodes

Forward-Backward BRD Decoder

- For BRD algorithm to be compatible with FB algorithm, a variant ECN is needed, called BRD-ECN.
- BRD-ECN composed of two sub-blocks and three input vectors as shown

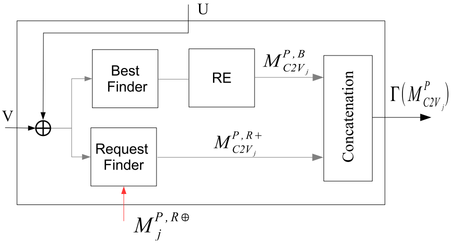

Figure 9: Structure of BRD-ECN

Forward-Backward BRD Decoder

- White ECN blocks → Conventional ECNs as in [5].
- Grey ECN blocks → BRD-ECNs.

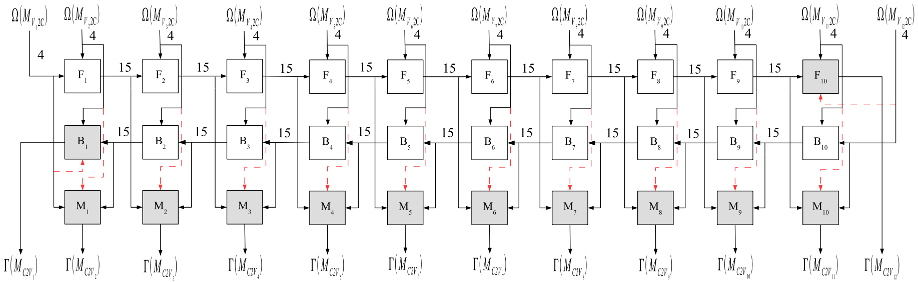

Figure 10: Forward-Backward BRD Architecture for $d_c = 12$

Complexity Analysis and Simulation Results

- Integrating BRD algorithm with FB algorithm reduces complexity of CN and VN units by reducing
  - Communication load.
  - Sorters size.
  - Arithmetic operations (real additions, GF additions, GF multiplications).
  - Memory Allocations.

Complexity Analysis and Simulation Results

Table 1: Size of Exchanged Messages per Edge on GF(64)

Scheme	Code Rate	Inputs		Outputs	
		$n_{vc}^{\oplus}$	n_{vc}^{+}	$n_{cv}^{\oplus}$	n_{cv}^{+}
FB-EMS[5]	any	20	19	20	19
FB-BRD	$r \geq 5/6$	4	3	4	6
	$r = 1/2$	8	7	6	10
	$r = 1/3$	13	12	7	14

Complexity Analysis and Simulation Results

- Hardware complexity of CN is studied using Quartus Prime synthesis tool.
- Fully-parallel implementation for a code rate $r = 5/6$ with $d_c = 12$ on Cyclone IV FPGA.
- FB-BRD algorithm reduces memory allocations by around 58% when compared with FB-EMS, and reduces computational complexity by around 15%.

Table 2: Synthesis Results for $d_c = 12$ on GF(64)

Scheme	Logic Elements	Registers
FB-EMS ($n_m = 16$) [5]	109860	89940
FB-BRD ($n_{vc} = 4, n_B = 4, n_R = 3$)	94782	37308

Complexity Analysis and Simulation Results

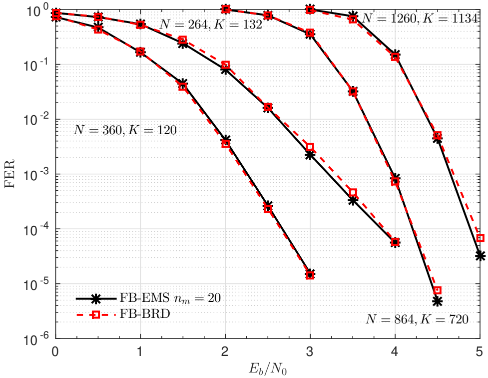

Figure 11: Simulation Results over GF(64) with AWGN and BPSK Modulation

Conclusion

- NB-LDPC Decoder suffers from high complexity.
- FB-BRD decoder allows for reducing the global complexity of the decoder.
- By allowing variable nodes to request reliability of specific symbols from the CN.
- Adaptation of BRD with FB approach requires novel ECN called BRD-ECN.
- Synthesis results of the check node with $d_c = 12$ show a complexity reduction of at least 15% in favor of the BRD-FB CN compared to the FB-EMS CN in terms of logic elements and 60% reduction in terms of memory allocations.
- Simulation results show no considerable performance loss for the FB-BRD tested at a FER down to 10^{-5} over different code rates and field orders.

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Thank You :)
Q & A?