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Interfaçage Logiciel

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Interfaçage Logiciel

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Plan

- Généralités sur la gestion des périphériques
- Les interruptions
- Un exemple

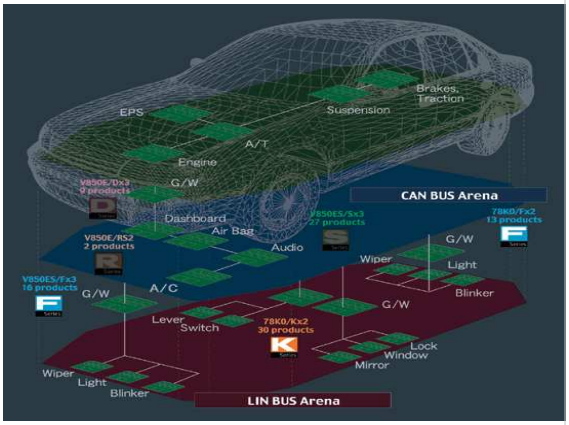
Généralités sur la gestion des périphériques

Généralités sur la gestion des périphériques

- Présentation du contexte : Les systèmes embarqués
- Qu'est-ce qu'un périphérique ?
- Interfaçage des périphérique

Les systèmes embarqués

- Systèmes au sein desquels des programmes de traitement complexes sont enfouis
  - Systèmes mixtes (info / elec)
  - Informatique
    - pas une fin mais un moyen



- Aujourd'hui les
  - véhicules
  - appareils ménagers
  - machines outils
  - robots mobiles

embarquent de l'informatique

Les systèmes embarqués

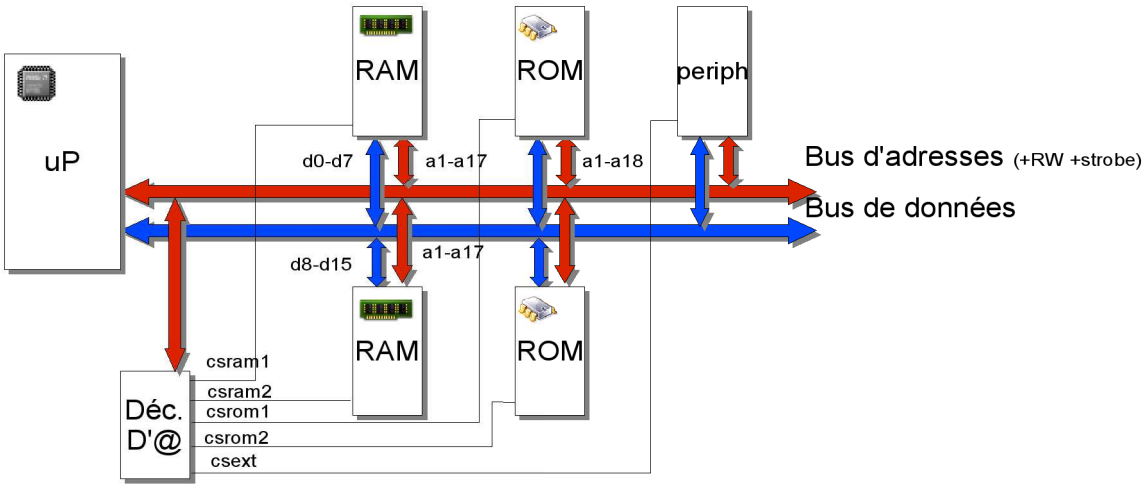
- Un ou plusieurs calculateurs (ECU) pour
  - Prendre des décisions
  - Appliquer les décisions

- Constitué de
  - Un ou plusieurs processeur
  - De la mémoire
  - Des entrées/sorties

- Les programmes informatiques fonctionnant sur le calculateur assurant la gestion du système

Rappels sur la constitution d'une carte micro

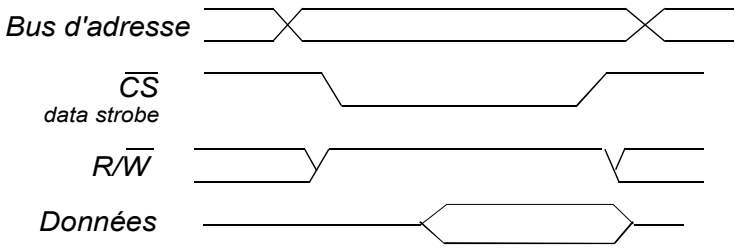
- Exemple d'une architecture 16 bits
  - 256ko RAM
  - 512ko Flash



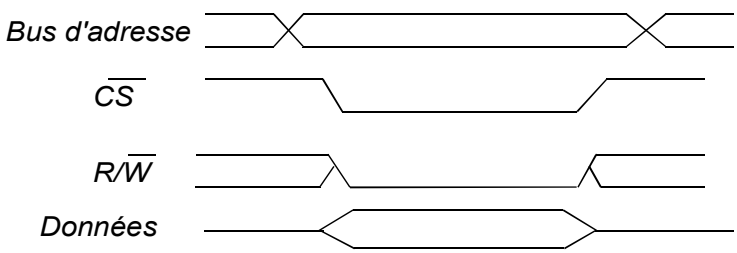
Rappels Cycles de Lecture / Ecriture

Sur un bus type 68000

- Lecture

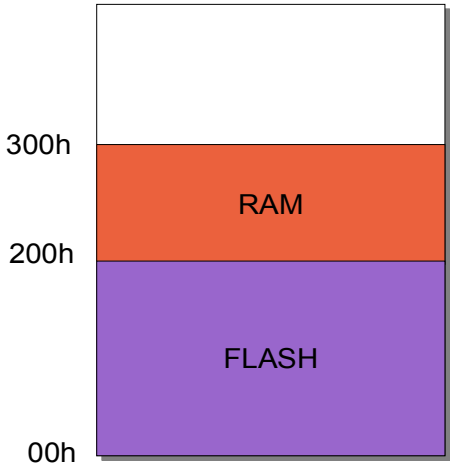


- Ecriture



Rappel
Mapping Mémoire, Décodage d'adresse

- Un espace d'adressage
- Chaque élément adressable en mémoire dispose d'une plage d'adresse
- Le décodeur d'adresse pilote le chip-select des périphérique suivant la plage visée par la requête



Exemple :
1 espace de 512ko (adressable sur 19bits)
1 espace de 256ko (adressable sur 18bits)
Les 19 bits de poids faibles permettent l'adressage dans le chip
Les bits de poids fort permet la sélection du chip
Le décodeur d'adresse sélectionne le chip grâce à ces bits

Qu'est-ce qu'un périphérique

- Les périphériques réalisent l'interface entre le processeur et le monde extérieur
- Ils sont interfaçés avec le processeur grâce au sous-système d'**entrées/sorties**
  - Directement sur le bus
  - Indirectement, à travers une liaison
    - Interface série
    - Interface parallèle
    - Réseau
- Certaines entrées/sorties intégrées dans le processeur : cas des *microcontrôleurs*

Exemples d'Entrée-Sorties

- Contrôleur réseau
- Contrôleur de Disque Dur
- UART
- PIA
- Interface moteur
  - Moteur DC
  - Moteur Pas à Pas
- Interface tout ou rien (entrée ou sortie)
- Interface capteurs analogiques
- Contrôleur clavier/souris
- Contrôleur Ecran

Interfaçage des périphériques
Cas des périphériques sur le bus

- Les périphériques qui sont sur le bus sont mappés dans l'espace adressable du processeur
- On les pilote grâce à des registres
  - On écrit en mémoire à l'adresse du périphérique
- Pour les périphériques 8bits
  - Attention avec les processeurs ayant un bus plus large
    - Sur 68000 : utilisation de l'instruction MOVEP

Interfaçage sur le bus
Exemple d'un PIA (Peripheral Interface Adapter)

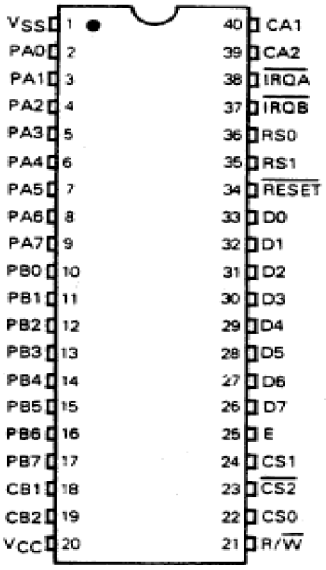
- MC6821
  - Permet d'interfacer des entrées/sorties sur le bus
  - 2 ports 8 bit (PA et PB)
    - Configurables en entrée ou sortie via le registre DDR
  - 4 pin d'interruption (CA / CB)

TABLE 1 – INTERNAL ADDRESSING

RS1	RS0	Control Register Bit CRA-2	Control Register Bit CRB-2	Location Selected
0	0	1	X	Peripheral Register A
0	0	0	X	Data Direction Register A
0	1	X	X	Control Register A
1	0	X	1	Peripheral Register B
1	0	X	0	Data Direction Register B
1	1	X	X	Control Register B

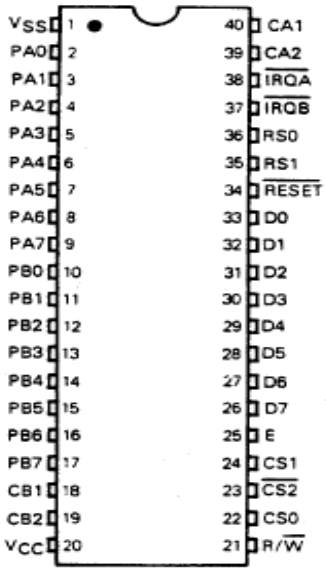
X = Don't Care

PIN ASSIGNMENT



Interfaçage sur le Bus
Exemple d'un PIA (bus timings)

PIN ASSIGNMENT

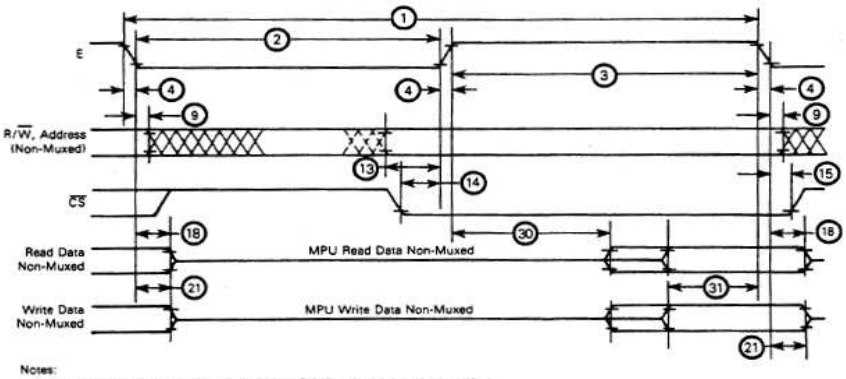


BUS TIMING CHARACTERISTICS (See Notes 1 and 2)

Ident. Number	Characteristic	Symbol	MC6821 Min	MC6821 Max	MC68A21 Min	MC68A21 Max	MC68B21 Min	MC68B21 Max	Unit
1	Cycle Time	t_{cyc}	1.0	10	0.67	10	0.5	10	µs
2	Pulse Width, E Low	PW_{EL}	430	–	280	–	210	–	ns
3	Pulse Width, E High	PW_{EH}	450	–	280	–	220	–	ns
4	Clock Rise and Fall Time	t_r, t_f	–	25	–	25	–	20	ns
9	Address Hold Time	t_{AH}	10	–	10	–	10	–	ns
13	Address Setup Time Before E	t_{AS}	80	–	60	–	40	–	ns
14	Chip Select Setup Time Before E	t_{CS}	80	–	60	–	40	–	ns
15	Chip Select Hold Time	t_{CH}	10	–	10	–	10	–	ns
18	Read Data Hold Time	t_{DHR}	20	50*	20	50*	20	50*	ns
21	Write Data Hold Time	t_{DHW}	10	–	10	–	10	–	ns
30	Output Data Delay Time	t_{DDR}	–	290	–	180	–	150	ns
31	Input Data Setup Time	t_{DSW}	165	–	80	–	60	–	ns

*The data bus output buffers are no longer sourcing or sinking current by t_{DHR}max (High Impedance).

FIGURE 1 – BUS TIMING



Notes:
1. Voltage levels shown are $V_L \leq 0.4$ V, $V_H \geq 2.4$ V, unless otherwise specified.
2. Measurement points shown are 0.8 V and 2.0 V, unless otherwise specified.

Interfaçage des E/S
Cas général

- On y accède à une E/S à travers un contrôleur
  - Directement sur le bus
  - via une interface série
    - RS232
    - I2C
    - SPI
    - USB
  - Ou un réseau / bus de terrain
    - Ethernet
    - CAN
  - Mais aussi parallèle
    - PCI
    - IDE

Topologies pour l'accès E/S

- Point à point
  - RS232
  - PIA
- Bus ou réseau
  - Permet de connecter plusieurs composants entre eux
  - USB
  - CAN
  - Ethernet
- Réseau sans fil
  - Wifi / bluetooth / zig-bee

Gestion logicielle

- Composants d'interfaçage => plusieurs protocoles
- Notion de pile de protocoles
- Gestion sous forme de librairies
- Si la plate-forme utilise un système d'exploitation (OS) alors on écrit des *pilotes de périphérique* pour chaque couche(driver)

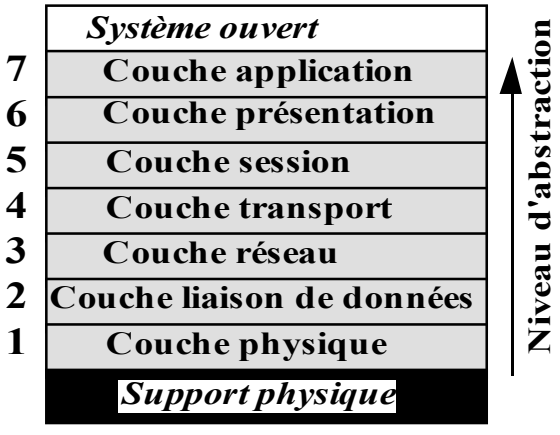
Gestion logicielle
Notion de Système d'Exploitation

- Peut être considéré comme une couche au dessus du processeur
- Il offre un certain nombre de services aux programmes utilisateur
  - Gestion de la mémoire
  - Abstraction des périphériques
  - Communication inter-processus
- Exemples d'OS
  - Unix/Linux, Windows, MS-DOS
  - VxWorks, RTEMS, RT-Linux, UCos : Temps Réel

- Il existe des réseaux pour différentes échelles

Distance entre processeurs	Localisation des processeurs	Exemple
0, 1 m	Un circuit imprimé	Machine à flots de données
1 m	Un ordinateur	Multiprocesseur
10 m	Une salle	
100 m	Un immeuble	Réseau métropolitain, MAN (Metropolitan Area Network)
1 km	Un campus	
10 km	Une ville	
100 km	Une région	Réseau longue distance, WAN (Wide Area Nertwork)
1000 km	Un continent	
10000 km	La terre entière	Internet

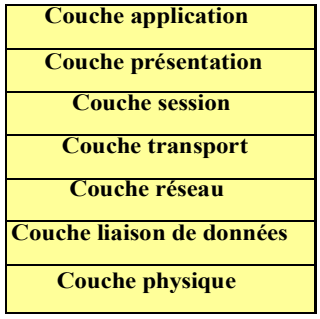
- Un réseau fournit plusieurs services aux applications
- Une pile de protocole a été normalisée
  - Pile **OSI**



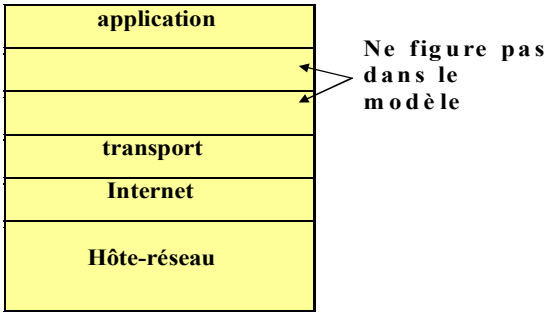
Pile OSI

Gestion logicielle
Passage au travers d'un réseau

- TCP/IP suit à peu près la pile OSI mais est antérieur

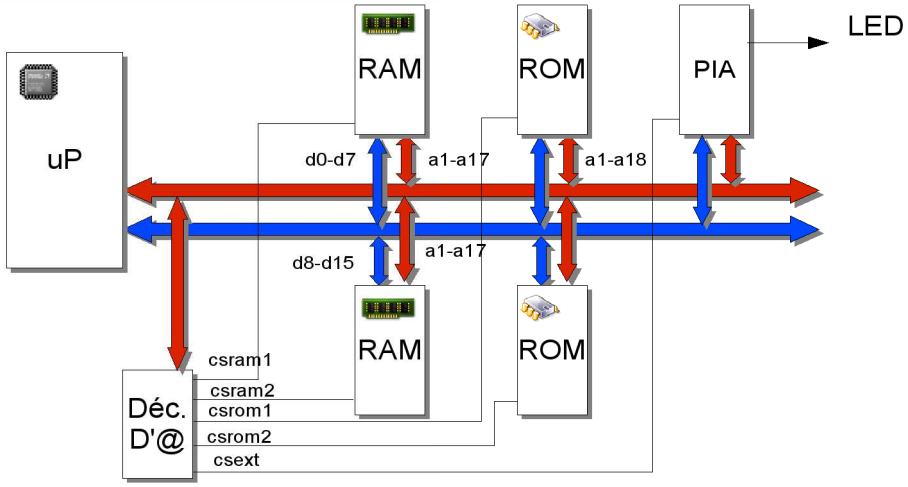


Modèle de référence OSI



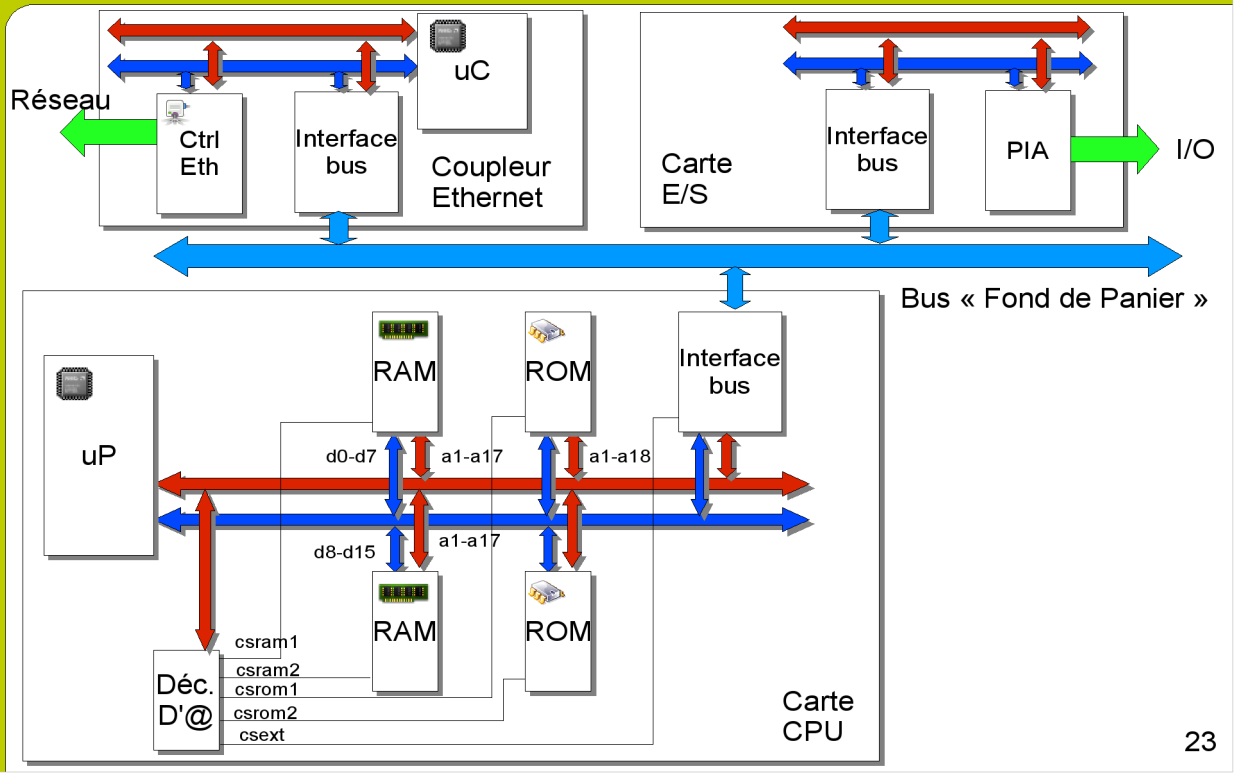
Modèle de référence TCP/IP

Exemple
Pilotage d'une LED



- On utilise un PIA (Parallel Interface Adapter)
- Nécessité de **configurer le PIA**
  - Un registre de direction (entrée / sortie) (DDR)
  - Un registre de contrôle
- Un troisième registre permet d'accéder au port

Exemple
Constitution d'un automate programmable



Résumé

- L'interfaçage consiste à gérer les périphériques autour d'un système embarqué
- Chaque périphérique apporte
  - ses contraintes mécaniques
  - ses contraintes d'interfaçage
  - ses contraintes logicielles
- Au niveau logiciel on peut être amené à implémenter plusieurs protocoles avant d'accéder à un périphérique

Gestion des interruptions

Plan

- Dialogue Périphérique <-> Micro
- Notion d'interruption
- Types d'interruptions
- Les interruptions au niveau logiciel

Le dialogue entre le périphérique et le micro

- Comment fais-t-on lorsqu'un périphérique prends du temps pour répondre à une requête ?
- Comment le périphérique peut-il envoyer une information au micro ?

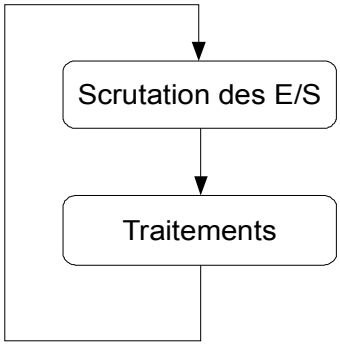
Le dialogue entre le périphérique et le micro

- Cas simple :
  - Le périphérique réponds directement au micro
  - S'applique uniquement si le traitement et la gestion d'E/S réalisés par le périphérique est rapide
  - Principalement pour les accès à des registres ou des mémoires
- Pour un périphérique plus lent que le processeur
  - Gestion **asynchrone** de la communication
    - Le processeur envoie une commande
    - Quand le périphérique a traité cette commande, il indique au processeur qu'il est prêt et renvoie son résultat
  - Le périphérique doit alors pouvoir indiquer au processeur qu'il est prêt

Le dialogue entre le périphérique et le micro

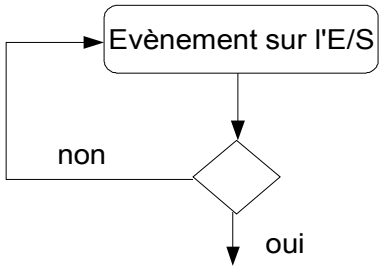
- **Méthode 1 :** La scrutation (ou polling)
  - Le programme interroge périodiquement le périphérique (lecture d'une broche ou d'un registre)

Cas 1 :



1. On examine les entrées sorties (non bloquant)
2. La réalisation des traitements dépends des E/S

Cas 2 : L'attente Active



- On attends un événement sur une E/S (bloquant)
- Dans le cas multi-tâche, il faut ajouter une attente

Exemple
Lecture d'une donnée sur un port série

- Contexte : enregistrement de trames NMEA
  - Une trame NMEA, ne peut être traitée que si elle est entièrement lue
  - Exemple de trame : *geographic position*

GLL-Geographic Position-Latitude/Longitude
Table B-4 contains the values for the following example:
$GPGLL,3723.2475,N,12158.3416,W,161229.487,A*2C

Table B-4 GLL Data Format

Name	Example	Units	Description
Message ID	$GPGLL		GLL protocol header
Latitude	3723.2475		ddmm.mmmm
N/S Indicator	n		N=north or S=south
Longitude	12158.3416		dddmm.mmmm
E/W Indicator	W		E=east or W=west
UTC Position	161229.487		hhmmss.sss
Status	A		A=data valid or V=data not valid
Checksum	*2C		
<CR><LF>			End of message termination

  - Au niveau de l'UART
    - Un bit DR (Data Ready) => caractère reçu
    - Un registre contenant la donnée (0x0)

Exemple
Lecture d'une donnée sur un port série

Programme de lecture des caractères

```
Boucler
  Boucler
  TantQue DR == 0 // Caractère reçu

  Lire caractère
  trame += caractère
TantQue Caractère != LF // Fin de trame

Traitement de la trame
```

On monopolise le processeur

Exemple
Ecriture d'une donnée sur un port série

Programme d'écriture des caractères

```
trame = ''Hello''

Pour i allant de 0 à longueur(trame)
  Boucler
  TantQue THRE == 0 // Buffer d'envoi libre
                    // on peut continuer
  envoyer (trame[i])

FPour
```

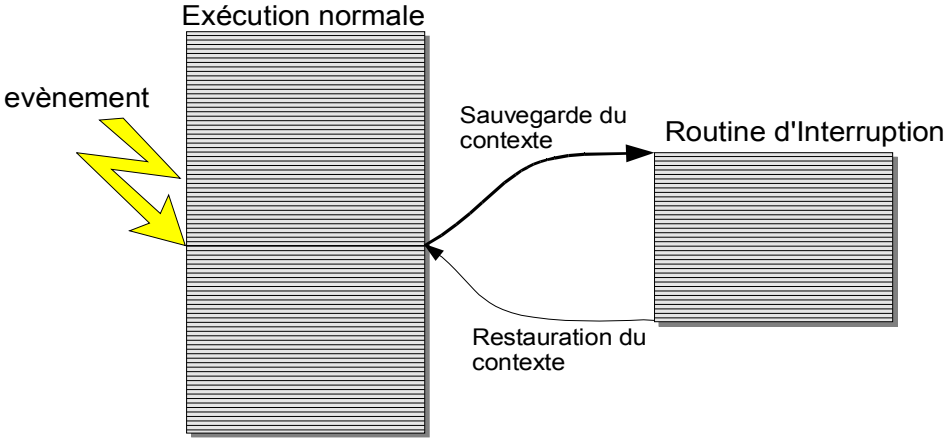
Le dialogue entre le périphérique et le micro

- Intérêt
  - Uniquement logiciel
  - Simple à mettre en oeuvre
- Inconvénients
  - Le processeur passe son temps à attendre les périphériques

Pourquoi le périphérique n'indiquerait-il pas au processeur qu'il a quelque-chose à dire ?

Notion d'interruption

- Mécanisme **Matériel** pour traiter la communication depuis le périphérique
- Le fonctionnement du programme est arrêté pour exécuter une routine particulière
  - Interrupt Service Routine (ISR)

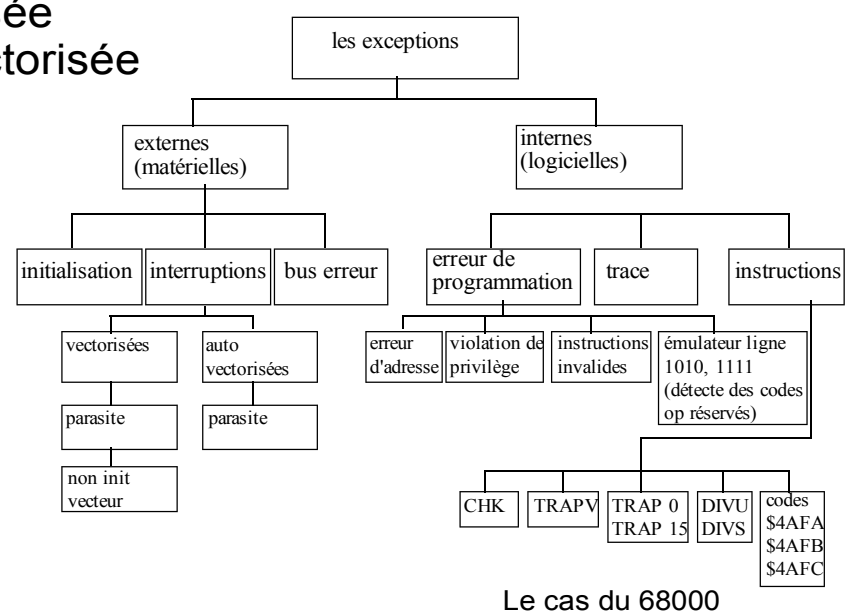


Interruptions fréquentes

- RTC (Real-Time Clock)
  - Gestion de l'horloge
- Contrôleur de disque
  - Accès aux données sur un support lent
- Réseau
- Liaison série
- Clavier / Boutons divers
- Capteurs
- ....

Typologie des interruptions

- Exception
- Interruption
  - Vectorisée
  - Autovectorisée



Le cas du 68000

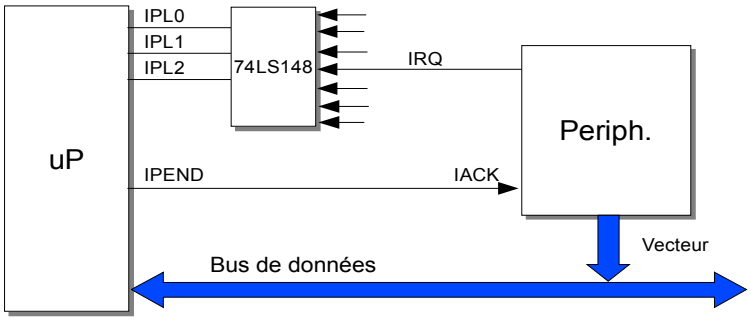
Interruptions Vectorisées
La notion de vecteur d'interruption

- Le **vecteur d'interruption** permet d'identifier le périphérique à l'origine de l'interruption
- La **table des exceptions** est ensuite utilisée pour dérouter le programme vers la bonne **ISR**
  - Une ligne pour chaque vecteur
  - Peut contenir l'adresse de l'ISR ou une instruction

- Cas du 68000
  - La table des vecteurs est située en 0x0
  - La première ligne (0x00) indique le pointeur de pile
  - La seconde ligne (0x04)indique le début du code

Interruptions Vectorisées
Gestion par les périphériques

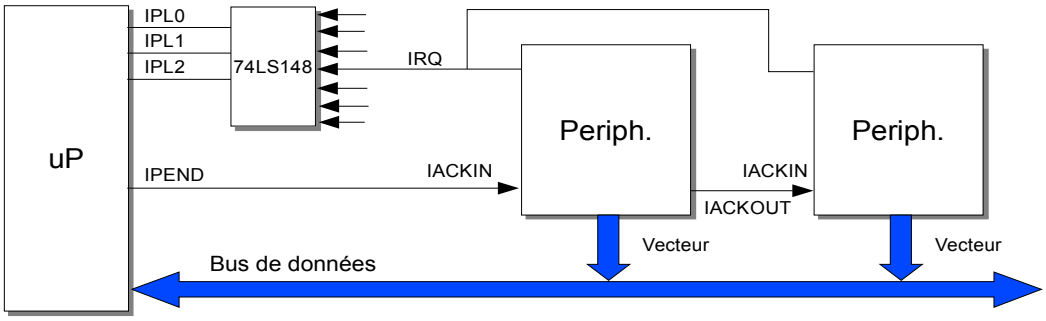
- Exemple du 68000
  - Utilisation d'un encodeur de priorité (de 0 à 7)
  - Priorité 7 : la plus forte (et **non masquable = NMI**)
  - Les périphériques envoient leur vecteur sur le Bus



  - Possibilité de chainer les périphériques sur un même niveau de priorité

Interruptions Vectorisées
Gestion par les périphériques (chaînage)

- Chaînage des périphériques
  - Notion de **Daisy Chain**



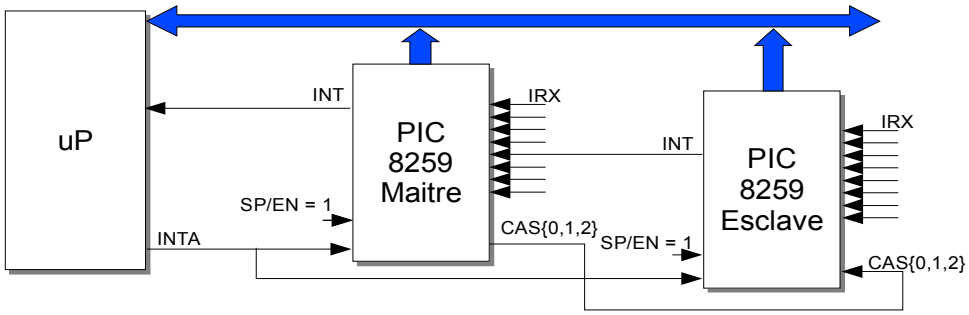
  - Si le périphérique n'est pas concerné, il fait suivre le signal IACK

Interruptions vectorisées
Contrôleur d'interruption PIC

- *Programmable Interrupt Controler*
- Interface entre le processeur et le périphérique
- Gestion des priorités
- Sur 68000
  - On peut utiliser un simple **encodeur de priorité**
  - Ou plus perfectionné MFP 68901 *(Multi Function Peripheral)*
    - Gère l'envoi du vecteur par le Bus
- Sur architecture 8088 (intel)
  - Contrôleur 8259A

Interruptions Vectorisées
Contrôleur d'interruption PIC (2)

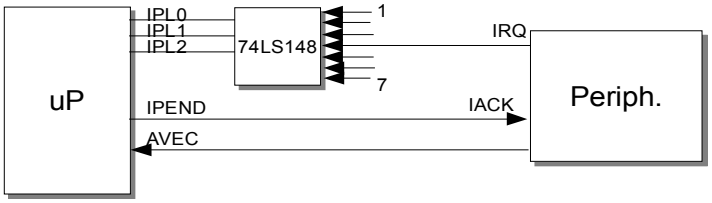
- Exemple d'Utilisation du PIC 8259A
  - La solution adoptée sur le PC
  - C'est le *PIC* qui renvoie l'adresse du périphérique
    - **Nécessité de le programmer**
  - 8 niveaux de priorité, possibilité de cascader les PIC



  - Les lignes CAS{0,1,2} permettent au maître d'indiquer quel esclave a reçu l'ack

Interruptions Auto-Vectorisées

- Simplifie au maximum la gestion des interruptions
- Tous les processeurs ne le gèrent pas
- <u>Exemple sur une archi. de type 68k :</u>



  - Le périphérique ou contrôleur génère un signal AVEC
    - On utilise l'autovecteur associé à l'IRQ4 (vecteur 25 + 4)
  - En reliant IPEND et AVEC
    - On limite le nombre d'interruptions extérieures à 7
    - On simplifie fortement la gestion des IT

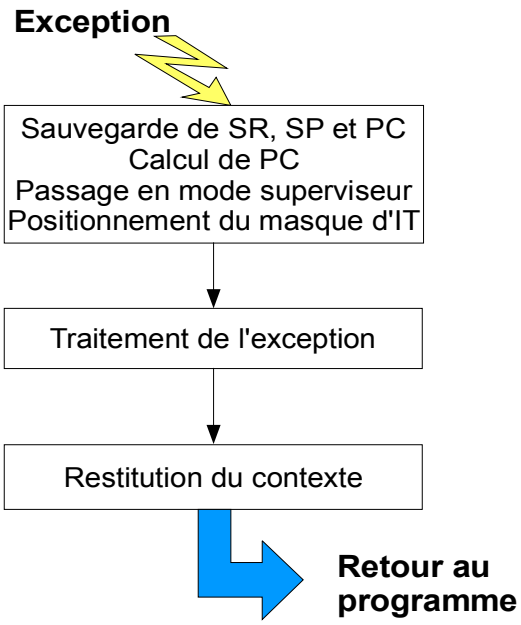
Interruptions Logicielles
Exceptions logicielles ou TRAP

- Exceptions logicielles
  - Permettent de traiter logiciellement un problème survenu sur l'archi
    - Ex : *Bus Error*, *Address Error*, *Divide By Zero*, *Instruction Coprocesseur*
  - On peut alors réagir et traiter le problème
- Les **TRAP**
  - Permettent de faire un appel système (passage en mode superviseur)
  - Certains OS réalisent leurs appels système par ce biais
    - Ex : MSDOS
      - 020h : fin d'un programme
      - 021h : gestion des périphériques
      - ...

Fonctionnement logiciel des interruptions

- Au niveau logiciel
  - En assembleur, une interruption est une routine
  - En C, on utilise une fonction
  - Le retour est différent d'une routine *normale*
    - **RTE** au lieu de RTS sur un 68000
    - **IRET** au lieu de RET sur un 8088
    - *Permet de traiter les aspects matériels de l'appel à l'IT*

Algorithme du traitement des exceptions sur un 68000



Ecriture d'une ISR

Exemple d'ISR :

```
SP_IT:
  MOVEM.L D0-D2/A4,-(A7)
 ...
 ...
  MOVEM.L (A7)+,D0-D2/A4
  RTE
```

- Bien sauvegarder les registres utilisés dans l'interruption et les restituer à la fin
- Notion de masquage
  - Pendant l'IT, les interruption de niveau inférieur ne peuvent être appelées
  - Par contre l'IT peut elle même être interrompue par une IT de niveau supérieur

Exemple de programme fonctionnant sous IT

- Pour la lecture des trames NMEA du GPS
  - L'ISR associée au port série peut enregistrer les trames dans un tableau

```
global var trame[]
global var ptrame

Routine interruption réception_série
  Lire caractère
  trame[ptrame] += caractère
  Si caractère == LF // Fin de trame
    ptrame++
  FSi
FRoutine
```


Exemple de programme fonctionnant sous IT

- Le programme principal n'a alors plus qu'à vérifier que le pointeur de trame aie été incrémenté pour traiter l'IT

```
var ptram_cur

Boucler
  Traitements divers

  Boucler // on attends une trame
  TantQue ptram_cur == ptram

  Traitement de trame[ptram_cur]
  ptram_cur ++
...
```

Exemple de programme fonctionnant sous IT

- Pour l'écriture sur le port série

```
Routine interruption emission_série
   Ecrire trame[ptrame]
   ptrame++
   Si trame[ptrame] == LF // Fin de trame
      inhiber emission_série
   FSi
Froutine
```

- Dans le programme principal

```
trame = message
activer emission_série
```


Avantages / Inconvénients

- Avantages
  - On peut faire tout un ensemble de traitements et recevoir les trames en parallèle
  - Gains en terme de performance
- Inconvénients
  - Conceptuellement plus compliqué
  - Plus difficile à débugger

Résumé

- Plusieurs façons de communiquer avec les périphériques de manière *asynchrone*
  - Par polling
  - En utilisant le mécanisme d'Interruptions
- Les interruptions sont un mécanisme matériel, fourni par le processeru
- Notion de contrôleur d'interruption (PIC)
- Notion de routine d'interruption (ISR)

Exemple complet

Introduction

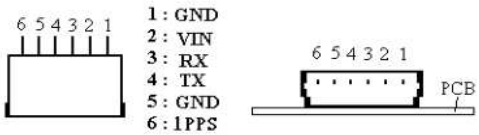
Les éléments intervenants dans l'interfaçage d'un GPS NMEA

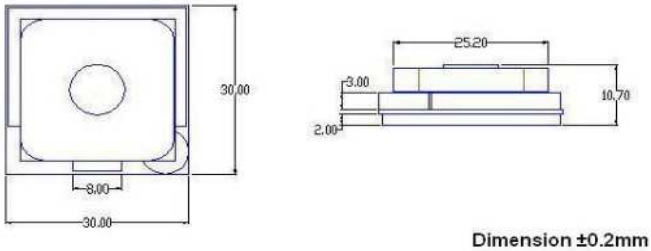
- Présentation du GPS NMEA
- Interfaçage matériel
- Structuration logicielle
- La gestion du GPS

Présentation du périphérique

- Dans la datasheet
  - Vérifier comment s'interface le périphérique

Protocol	
Electrical level	TTL level, Output voltage level: 0V ~ 2.85V
	RS-232 level
Baud rate	4,800 bps
Output message	NMEA 0183 GGA, GSA, GSV, RMC, VTG, GLL





Dimension ±0.2mm

Présentation du périphérique
Protocole : Exemple de commande

- Protocole du GPS
  - Commande

A). Set Serial Port ID:100 Set PORTA parameters and protocol

This command message is used to set the protocol(SiRF Binary, NMEA, or USER1) and/or the communication parameters(baud, data bits, stop bits, parity). Generally,this command would be used to switch the module back to SiRF Binary protocol mode where a more extensive command message set is available. For example,to change navigation parameters. When a valid message is received,the parameters will be stored in battery backed SRAM and then the receiver will restart using the saved parameters.

Format:

$PSRF100,<protocol>,<baud>,<DataBits>,<StopBits>,<Parity>*CKSUM
<CR><LF>

<protocol>	0=SiRF Binary, 1=NMEA, 4=USER1
<baud>	1200, 2400, 4800, 9600, 19200, 38400
<DataBits>	8,7. Note that SiRF protocol is only valid f8 Data bits
<StopBits>	0,1
<Parity>	0=None, 1=Odd, 2=Even

Example 1: Switch to SiRF Binary protocol at 9600,8,N,1
$PSRF100,0,9600,8,1,0*0C<CR><LF>

Présentation du périphérique
Protocole : Exemple de donnée reçue

- Exemple de trames NMEA reçue
  - GLL : renvoie la position courante

GLL-Geographic Position-Latitude/Longitude

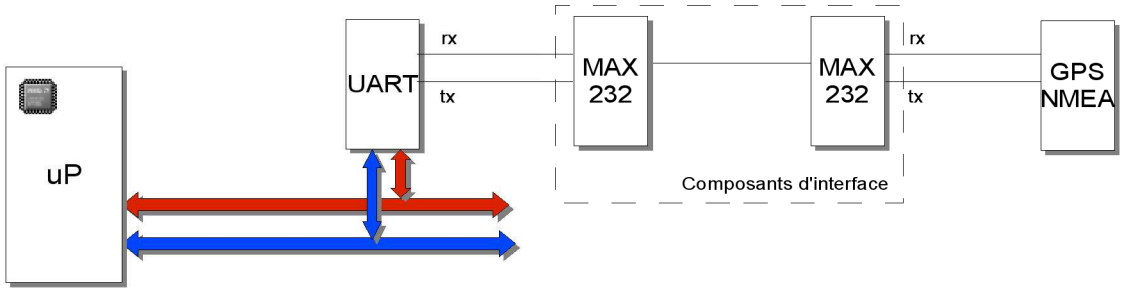
Table B-4 contains the values for the following example:

$GPGLL,3723.2475,N,12158.3416,W,161229.487,A*2C

Table B-4 GLL Data Format

Name	Example	Units	Description
Message ID	$GPGLL		GLL protocol header
Latitude	3723.2475		ddmm.mmmm
N/S Indicator	n		N=north or S=south
Longitude	12158.3416		dddmm.mmmm
E/W Indicator	W		E=east or W=west
UTC Position	161229.487		hhmmss.sss
Status	A		A=data valid or V=data not valid
Checksum	*2C		
<CR><LF>			End of message termination

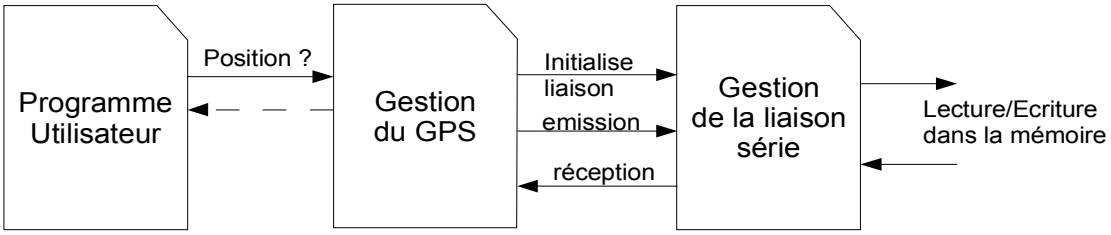
Interfaçage matériel



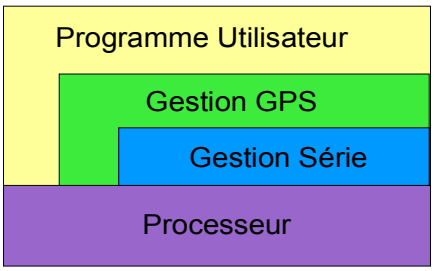
- Le GPS est connecté sur un port série (RS232)
- Il faut donc gérer la connexion au port série avant d'écrire le code pour gérer le GPS
- (on ne tient pas compte de la broche pps dans l'exemple)

Structure du logiciel

- Appel des différents sous-programmes nécessaire à la communication avec le GPS



- Pile de protocoles
  - Le service des couches supérieures reposent sur ceux fournis par les couches en dessous



Gestion de la liaison série

- Le code de gestion du port série doit permettre
  - De fixer les paramètres d'émission/réception
  - D'émettre des données sur la liaison
  - De recevoir des données
- L'interface doit être la plus simple possible
  - Parametres (params)
  - Emmettre (données)
  - Recevoir
- On choisit de réaliser une gestion par interruption

Pilotage du GPS

- Il faut assurer
  - La configuration et la communication avec le module GPS
  - La mise à disposition des données au programme de l'utilisateur
- Trouver une interface
  - Entre le programme Utilisateur et le pilote du GPS
    - De quelles informations le programme a-t-il besoin ?
    - Dans quel format ?

Données à récupérer

- Prenons l'exemple d'un *logiciel de navigation*
- L'application souhaite récupérer
  - la position
  - la vitesse au sol
- Le pilote du GPS lui fournira les fonctions
  - GetPosition
  - GetGroundSpeed
- A chaque appel à l'une de ces fonctions, le pilote du GPS
  - Récupérera les trames reçues à travers la liaison série
  - Retournera la dernière valeur reçue

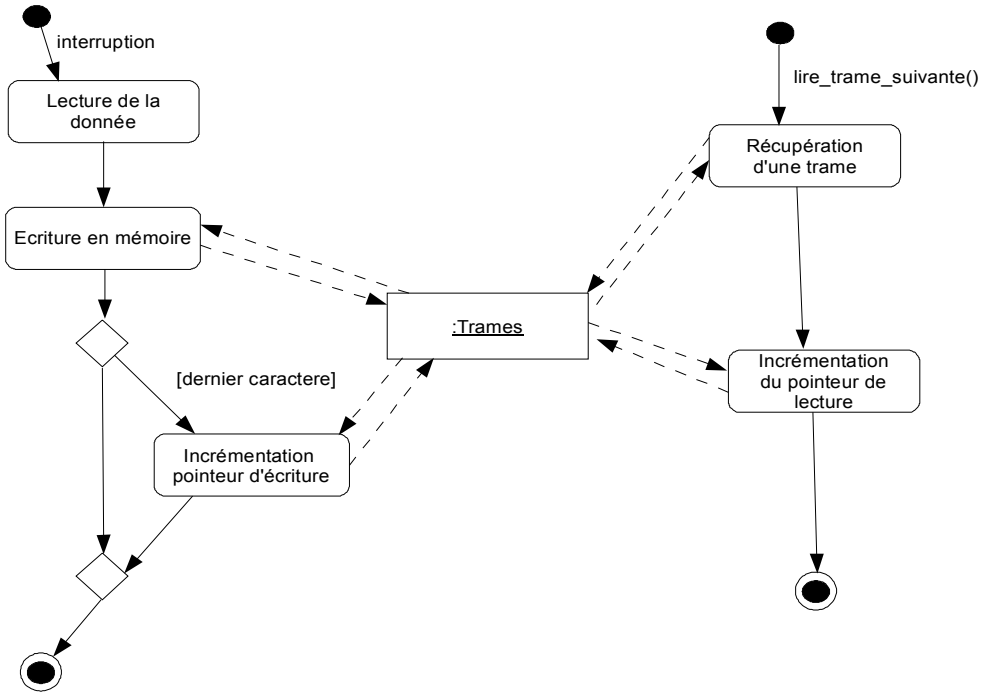
Variations

- On peut concevoir des variations
  - Un pilote du GPS avec un fonctionnement périodique
    - Développement d'une interruption *timer* stockant les données reçues dans un tableau
    - Pas facile à mettre au point
    - Plus simple dans un contexte multi-tâche
  - Une version du pilote de la gestion série *couplée finement* avec le pilote du GPS
    - L'interruption de réception série commence la traduction des trames NMEA
    - Le pilote série devient spécifique

Réalisation logicielle
Mécanisme de lecture sur le port série

- Les données sont
  - Reçues par l'interruption
  - Placées dans un buffer sous forme de tableau
- Deux compteurs sont utilisés
  - Dernière trame écrite (par l'interruption)
  - Dernière trame lue (par le programme)
  - Compteurs *modulo N*
- Deux routines sont fournies
  - lire_trame_suivante
    - Renvoie la trame suivante
    - Bloque si les deux compteurs sont égaux
  - test_trame
    - Indique s'il de nouvelles trames ont été reçues
    - Un test sur les pointeurs ...

Réalisation logicielle
Mécanisme de lecture sur le port série



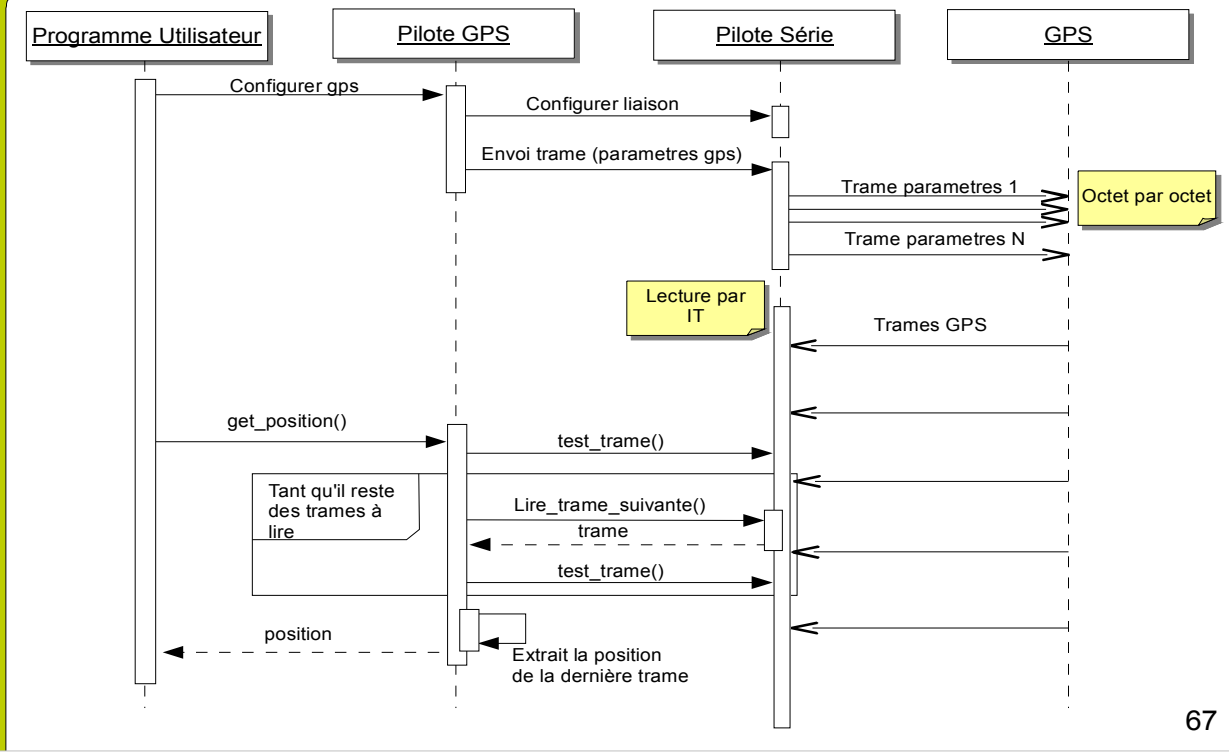
Réalisation logicielle
Ecriture sur le port série

- Une routine est fournie au programme utilisateur
  - envoyer_trame_serie
  - Place la trame dans un buffer (même organisation que pour la lecture)
  - Lance l'interruption
- La routine d'interruption
  - Envoie les trames caractère par caractère
  - Se désactive quand aucune trame n'est à envoyer

Réalisation logicielle
Récupérer la position

- Lit toutes les trames reçues par le port série
- Enregistre la dernière position connue (dernière trame GGL)
- Renvoie la dernière position connue au programme appelant

Exemple de communication



Datasheets

Vous trouverez dans cette section les datasheet de quelques périphériques évoqués dans le cours :

- PC16450 (8250) : Une UART
- MC6821 : Un PIA
- 8259A : Le Contrôleur d'interruptions Intel
- EM406A : Le récepteur GPS étudié dans l'exemple

National Semiconductor

July 1990

PC16450C/NS16450, PC8250A/INS8250A Universal Asynchronous Receiver/Transmitter

General Description

This part functions as a serial data input/output interface in a microcomputer system. The system software determines the functional configuration of the UART via a TRI-STATE® 8-bit bidirectional data bus.

The UART performs serial-to-parallel conversion on data characters received from a peripheral device or a MODEM, and parallel-to-serial conversion on data characters received from the CPU. The CPU can read the complete status of the UART at any time during the functional operation. Status information reported includes the type and condition of the transfer operations being performed by the UART, as well as any error conditions (parity, overrun, framing, or break interrupt).

The UART includes a programmable baud rate generator that is capable of dividing the timing reference clock input by divisors of 1 to $(2^{16}-1)$, and producing a 16 × clock for driving the internal transmitter logic. Provisions are also included to use this 16 × clock to drive the receiver logic. The UART includes a complete MODEM-control capability and a processor-interrupt system. Interrupts can be programmed to the user's requirements, minimizing the computing required to handle the communications link.

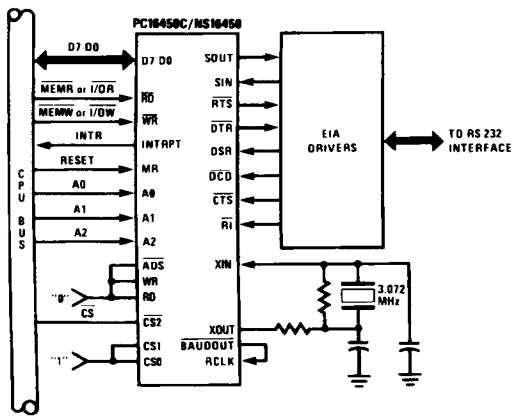
The PC16450C/NS16450 is an improved specification version of the PC8250C/INS8250-B Universal Asynchronous Receiver/Transmitter (UART). The UART is fabricated using National Semiconductor's advanced 1.25 μ CMOS process.

The PC16450C/NS16450 is functionally equivalent to the original NS16450, INS8250A, NS16C450 and INS82C50A, except that it has improved AC timing specifications and it is CMOS.

Features

- Easily interfaces to most popular microprocessors.
- Adds or deletes standard asynchronous communication bits (start, stop, and parity) to or from serial data stream.
- Holding and shift registers eliminate the need for precise synchronization between the CPU and the serial data.
- Independently controlled transmit, receive, line status, and data set interrupts.
- Programmable baud generator allows division of any input clock by 1 to $(2^{16}-1)$ and generates the internal 16 × clock.
- Independent receiver clock input.
- MODEM control functions (CTS, RTS, DSR, DTR, RI, and DCD).
- Fully programmable serial-interface characteristics:
  - 5-, 6-, 7-, or 8-bit characters
  - Even, odd, or no-parity bit generation and detection
  - 1-, 1½-, or 2-stop bit generation
  - Baud generation (DC to 256 kbaud)
- False start bit detection.
- Complete status reporting capabilities.
- TRI-STATE TTL drive capabilities for bidirectional data bus and control bus.
- Line break generation and detection.
- Internal diagnostic capabilities:
  - Loopback controls for communications link fault isolation
  - Break, parity, overrun, framing error simulation.
- Fully prioritized interrupt system controls.

Connection Diagram



TL/C/8401–1

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RRD-B20M70/Printed in U. S. A.

Table of Contents

1.0 Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Temperature Under Bias	0°C to +70°C
Storage Temperature	−65°C to +150°C
All Input or Output Voltages with Respect to V_{SS}	−0.5V to +7.0V
Power Dissipation	700 mW

Note: *Maximum ratings indicate limits beyond which permanent damage may occur. Continuous operation at these limits is not intended and should be limited to those conditions specified under DC electrical characteristics.*

2.0 DC Electrical Characteristics

T_A = 0°C to +70°C, V_{DD} = +5V ±10%, V_{SS} = 0V, unless otherwise specified.

Symbol	Parameter	Conditions	PC16450C/NS16450		PC8250A/INS8250A		Units
			Min	Max	Min	Max	
V_{ILX}	Clock Input Low Voltage		−0.5	0.8	−0.5	0.8	V
V_{IHX}	Clock Input High Voltage		2.0	V_{DD}	2.0	V_{DD}	V
V_{IL}	Input Low Voltage		−0.5	0.8	−0.5	0.8	V
V_{IH}	Input High Voltage		2.0	V_{DD}	2.0	V_{DD}	V
V_{OL}	Output Low Voltage	I_{OL} = 1.6 mA on all (Note 2)		0.4		0.4	V
V_{OH}	Output High Voltage	I_{OH} = −1.0 mA (Note 2)	2.4		2.4		V
I_{CC}(AV)	Avg. Power Supply Current	V_{DD} = 5.5V, T_A = 25°C No Loads on output SIN, DSR, DCD, CTS, RI = 2.4V All other inputs = 0.4V XIN = 8 MHz Divisor = EFFF		10		10	mA
I_{IL}	Input Leakage	V_{DD} = 5.5V, V_{SS} = 0V All other pins floating. V_{IN} = 0V, 5.5V		±10		±10	μA
I_{CL}	Clock Leakage			±10		±10	μA
I_{OZ}	TRI-STATE Leakage	V_{DD} = 5.5V, V_{SS} = 0V V_{OUT} = 0V, 5.5V 1) Chip deselected 2) WRITE mode, chip selected		±20		±20	μA
V_{ILMR}	MR Schmitt V_{IL}			0.8		0.8	V
V_{IHMR}	MR Schmitt V_{IH}		2.0		2.0		V

Capacitance T_A = 25°C, V_{DD} = V_{SS} = 0V

Symbol	Parameter	Conditions	Min	Typ	Max	Units
C_{IN}	Input Capacitance	f_c = 1		6	10	pF
C_{OUT}	Output Capacitance	Unmeasured pins returned to V_{SS}		10	20	pF
$C_{I/O}$	Input/Output Capacitance			10	12	pF

3.0 AC Electrical Characteristics $T_A = 0°C$ to $+70°C$, $V_{DD} = +5V \pm 10\%$

Symbol	Parameter	Conditions	PC16450C/NS16450		PC8250A/INS8250A		Units
			Min	Max	Min	Max	
t_{ADS}	Address Strobe Width		25		60		ns
t_{AH}	Address Hold Time		0		0		ns
t_{AR}	RD, $\overline{RD}$ Delay from Address	(Note 1)	20		30		ns
t_{AS}	Address Setup Time		25		60		ns
t_{AW}	WR, $\overline{WR}$ Delay from Address	(Note 1)	20		30		ns
t_{CH}	Chip Select Hold Time		0		0		ns
t_{CS}	Chip Select Setup Time		25		60		ns
t_{CSC}	Chip Select Output Delay from Select	@100 pF loading (Note 1)		33		45	ns
t_{CSR}	RD, $\overline{RD}$ Delay from Chip Select	(Note 1)	20		30		ns
t_{CSW}	WR, $\overline{WR}$ Delay from Select	(Note 1)	20		30		ns
t_{DH}	Data Hold Time		10		30		ns
t_{DS}	Data Setup Time		20		30		ns
t_{HZ}	RD, $\overline{RD}$ to Floating Data Delay	@100 pF loading (Note 3)	0	25	0	100	ns
t_{MR}	Master Reset Pulse Width		500		500		ns
t_{RA}	Address Hold Time from RD, $\overline{RD}$	(Note 1)	0		0		ns
t_{RC}	Read Cycle Delay		36		125		ns
t_{RCS}	Chip Select Hold Time from RD, $\overline{RD}$	(Note 1)	0		20		ns
t_{RD}	RD, $\overline{RD}$ Strobe Width		60		125		ns
t_{RDD}	RD, $\overline{RD}$ to Driver Disable Delay	@100 pF loading (Note 3)		20		60	ns
t_{RVD}	Delay from RD, $\overline{RD}$ to Data	@100 pF loading		31		60	ns
t_{WA}	Address Hold Time from WR, $\overline{WR}$	(Note 1)	0		0		ns
t_{WC}	Write Cycle Delay		36		150		ns
t_{WCS}	Chip Select Hold Time from WR, $\overline{WR}$	(Note 1)	0		0		ns
t_{WR}	WR, $\overline{WR}$ Strobe Width		60		100		ns
t_{XH}	Duration of Clock High Pulse	External Clock (8.0 MHz Max.)	55		55		ns
t_{XL}	Duration of Clock Low Pulse	External Clock (8.0 MHz Max.)	55		55		ns
RC	Read Cycle = $t_{AR} + t_{RD} + t_{RC}$		115		280		ns
WC	Write Cycle = $t_{AW} + t_{WR} + t_{WC}$		115		280		ns
Baud Generator							
N	Baud Divisor		1	$2^{16}-1$	1	$2^{16}-1$	
t_{BHD}	Baud Output Positive Edge Delay	100 pF Load		175		175	ns
t_{BLD}	Baud Output Negative Edge Delay	100 pF Load		175		175	ns
t_{HW}	Baud Output Up Time	$f_X = 8.0$ MHz, ÷2, 100 pF Load	100		100		ns
t_{LW}	Baud Output Down Time	$f_X = 8.0$ MHz, ÷2, 100 pF Load	100		100		ns
Receiver							
t_{RINT}	Delay from RD, $\overline{RD}$ (RD RBR or RD LSR) to Reset Interrupt	100 pF Load		40		1000	ns
t_{SCD}	Delay from RCLK to Sample Time			33		2000	ns
t_{SINT}	Delay from Stop to Set Interrupt			2		1	RCLK Cycles (Note 2)

Note 1: Applicable only when $\overline{ADS}$ is tied low.

Note 2: RCLK is equal to t_{XH} and t_{XL}.

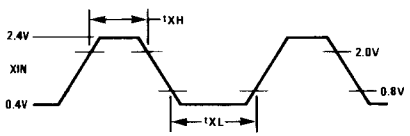
Note 3: Charge and discharge time is determined by V_{OL}, V_{OH} and the external loading.

3.0 AC Electrical Characteristics $T_A = 0°C$ to $+70°C$, $V_{DD} = +5V \pm 10\%$ (Continued)

Symbol	Parameter	Conditions	PC16450C/NS16450		PC8250A/INS8250A		Units
			Min	Max	Min	Max	
Transmitter							
t_{HR}	Delay from WR, $\overline{WR}$ (WR THR) to Reset Interrupt	100 pF Load		40		175	ns
t_{IR}	Delay from RD, $\overline{RD}$ (RD IIR) to Reset Interrupt (THRE)	100 pF Load		40		250	ns
t_{IRS}	Delay from Initial INTR Reset to Transmit Start		8	24	8	24	BAUDOUT Cycles
t_{SI}	Delay from Initial Write to Interrupt		16	24	16	24	BAUDOUT Cycles
t_{STI}	Delay from Stop to Interrupt (THRE)			8		8	BAUDOUT Cycles
Modem Control							
t_{MDO}	Delay from WR, $\overline{WR}$ (WR MCR) to Output	100 pF Load		40		200	ns
t_{RIM}	Delay to Reset Interrupt from RD, $\overline{RD}$ (RD MSR)	100 pF Load		78		250	ns
t_{SIM}	Delay to Set Interrupt from MODEM Input	100 pF Load		40		250	ns

4.0 Timing Waveforms (All timings are referenced to valid 0 and valid 1)

External Clock Input (24 MHz Max.)



TL/C/8401-2

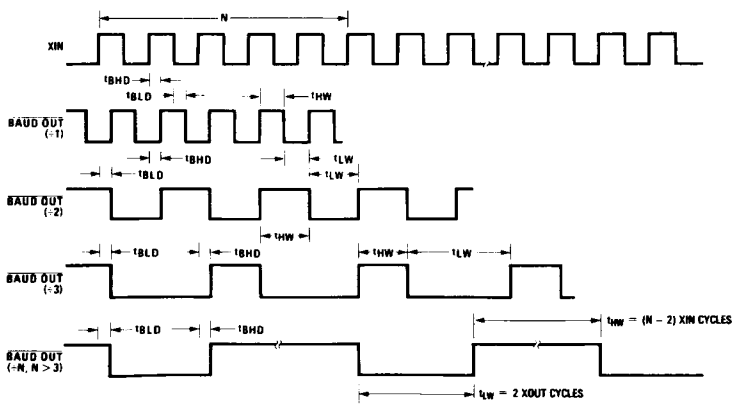
AC Test Points

TL/C/8401-3

Note 3: The 2.4V and 0.4V levels are the voltages that the inputs are driven to during AC testing.

Note 4: The 2.0V and 0.8V levels are the voltages at which the timing tests are made.

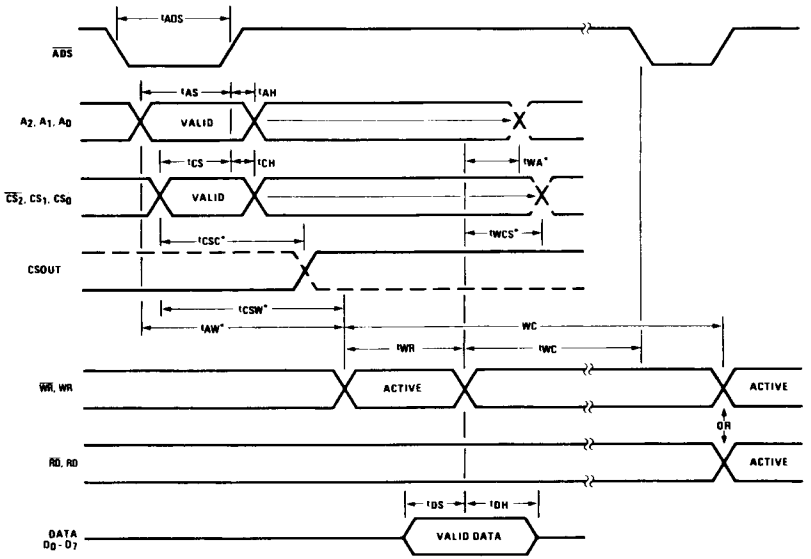
$\overline{BAUDOUT}$ Timing



TL/C/8401-4

4.0 Timing Waveforms (Continued)

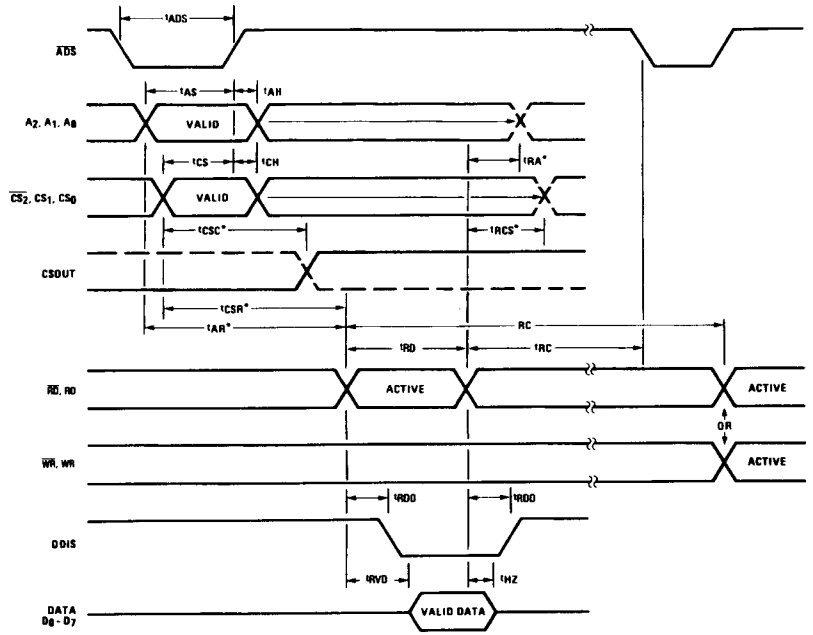
Write Cycle



*Applicable Only When $\overline{ADS}$ is Tied Low.

TL/C/8401-5

Read Cycle

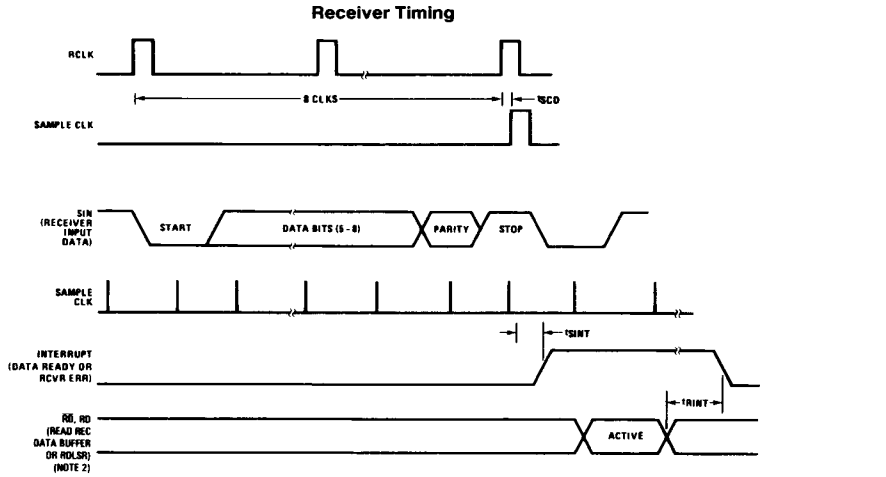


*Applicable Only When $\overline{ADS}$ is Tied Low.

TL/C/8401-6

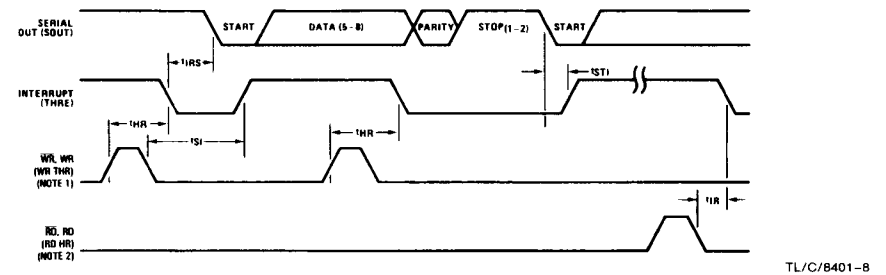
4.0 Timing Waveforms (Continued)

Receiver Timing



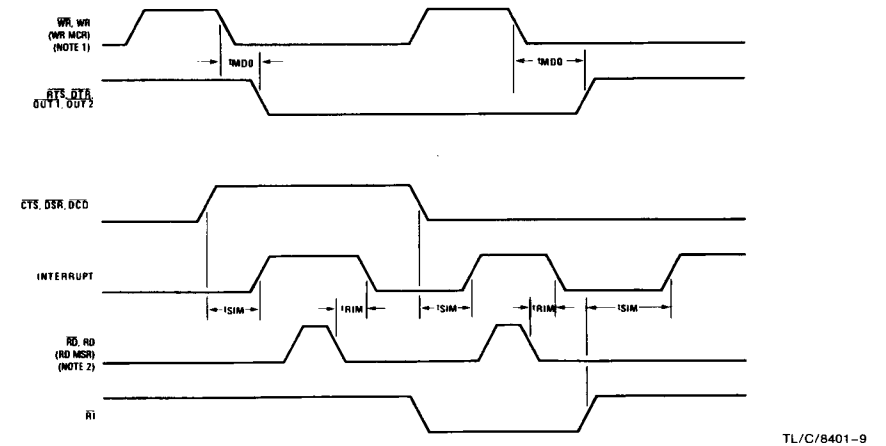
TL/C/8401-7

Transmitter Timing



TL/C/8401-8

MODEM Controls Timing

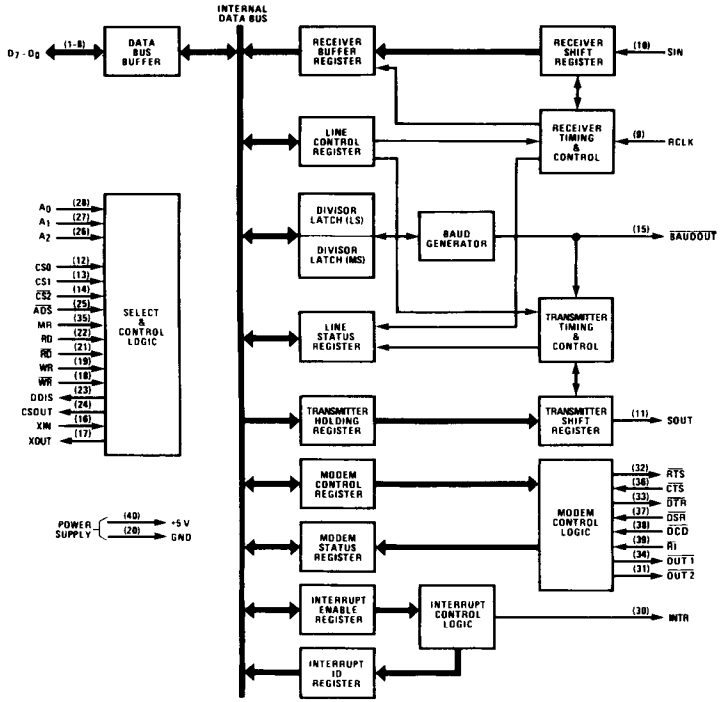


TL/C/8401-9

Note 1: See Write Cycle Timing

Note 2: See Read Cycle Timing

5.0 Block Diagram



TL/C/8401–10

Note: Applicable pinout numbers are included within parenthesis.

6.0 Pin Descriptions

The following describes the function of all UART pins. Some of these descriptions reference internal circuits.

In the following descriptions, a low represents a logic 0 (0V nominal) and a high represents a logic 1 (+2.4V nominal).

A0, A1, A2: Register Select Pins 26–28: Address signals connected to these 3 inputs select a UART register for the CPU to read from or write to during data transfer. The Register Addresses table associates these address inputs with the register they select. Note that the state of the Divisor Latch Access Bit (DLAB), which is the most significant bit of the Line Control Register, affects the selection of certain UART registers. The DLAB must be set high by the system software to access the Baud Generator Divisor Latches.

$\overline{\text{ADS}}$: Address Strobe Pin 25: The positive edge of an active Address Strobe ($\overline{\text{ADS}}$) signal latches the Register Select (A0, A1, A2) and Chip Select (CS0, CS1, CS2) signals.

Note: An active $\overline{\text{ADS}}$ input is required when the Register Select (A0, A1, A2) signals are not stable for the duration of a read or write operation. If not required, tie the $\overline{\text{ADS}}$ input permanently low.

$\overline{\text{BAUDOUT}}$: Baud Out Pin 15: This is the 16 × clock signal from the transmitter section of the UART. The clock rate is equal to the main reference oscillator frequency divided by the specified divisor in the Baud Generator Divisor Latches. The $\overline{\text{BAUDOUT}}$ may also be used for the receiver section by tying this output to the RCLK input of the chip.

Register Addresses

DLAB	A_2	A_1	A_0	Register
0	0	0	0	Receiver Buffer (read), Transmitter Holding Register (write)
0	0	0	1	Interrupt Enable
X	0	1	0	Interrupt Identification (read only)
X	0	1	1	Line Control
X	1	0	0	MODEM Control
X	1	0	1	Line Status
X	1	1	0	MODEM Status
X	1	1	1	Scratch
1	0	0	0	Divisor Latch (least significant byte)
1	0	0	1	Divisor Latch (most significant byte)

6.0 Pin Descriptions (Continued)

CS0, CS1, $\overline{CS2}$: Chip Select Pins 12–14: When CS0 and CS1 are high and $\overline{CS2}$ is low, the chip is selected. This enables communication between the UART and the CPU. The positive edge of an active Address Strobe signal latches the decoded chip select signals, completing chip selection. If $\overline{ADS}$ is always low, valid chip selects should stabilize according to the t_{CSW} parameter.

CSOUT: Chip Select Out Pin 24: When high, it indicates that the chip has been selected by active, CS0, CS1, and $\overline{CS2}$ inputs. No data transfer can be initiated until the CSOUT signal is a logic 1. CSOUT goes low when the UART is deselected.

$\overline{CTS}$: Clear to Send Pin 36: When low, this indicates that the MODEM or data set is ready to exchange data. The $\overline{CTS}$ signal is a MODEM status input whose conditions can be tested by the CPU reading bit 4 (CTS) of the MODEM Status Register. Bit 4 is the complement of the $\overline{CTS}$ signal. Bit 0 (DCTS) of the MODEM Status Register indicates whether the $\overline{CTS}$ input has changed state since the previous reading of the MODEM Status Register. $\overline{CTS}$ has no effect on the Transmitter.

Note: Whenever the CTS bit of the MODEM Status Register changes state, an interrupt is generated if the MODEM Status Interrupt is enabled.

D_7–D_0: Data Bus, Pins 1–8: This bus is comprised of eight TRI-STATE input/output lines. The bus provides bidirectional communications between the UART and the CPU. Data, control words, and status information are transferred via the D_7–D_0 Data Bus.

$\overline{DCD}$: Data Carrier Detect Pin 38: When low, indicates that the data carrier has been detected by the MODEM or data set. The $\overline{DCD}$ signal is a MODEM status input whose condition can be tested by the CPU reading bit 7 (DCD) of the MODEM Status Register. Bit 7 is the complement of the $\overline{DCD}$ signal. Bit 3 (DDCD) of the MODEM Status Register indicates whether the $\overline{DCD}$ input has changed state since the previous reading of the MODEM Status Register. $\overline{DCD}$ has no effect on the receiver.

Note: Whenever the DCD bit of the MODEM Status Register changes state, an interrupt is generated if the MODEM Status Interrupt is enabled.

DDIS: Driver Disable Pin 23: This goes low whenever the CPU is reading data from the UART. It can disable or control the direction of a data bus transceiver between the CPU and the UART (see Typical Interface for a High Capacity Data Bus).

$\overline{DSR}$: Data Set Ready Pin 37: When low, this indicates that the MODEM or data set is ready to establish the communications link with the UART. The $\overline{DSR}$ signal is a MODEM status input whose condition can be tested by the CPU reading bit 5 (DSR) of the MODEM Status Register. Bit 5 is the complement of the $\overline{DSR}$ signal. Bit 1 (DDSR) of the MODEM Status Register indicates whether the $\overline{DSR}$ input has changed state since the previous reading of the MODEM Status Register.

Note: Whenever the DSR bit of the MODEM Status Register changes state, an interrupt is generated if the MODEM Status Interrupt is enabled.

$\overline{DTR}$: Data Terminal Ready Pin 33: When low, this informs the MODEM or data set that the UART is ready to establish a communications link. The $\overline{DTR}$ output signal can be set to an active low by programming bit 0 (DTR) of the MODEM Control Register to a high level. A Master Reset operation sets this signal to its inactive (high) state. Loop mode operation holds this signal in its inactive state.

INTR: Interrupt Pin 30: This goes high whenever any one of the following interrupt types has an active high condition and is enabled via the IER: Receiver Line Status; Received Data Available; Transmitter Holding Register Empty; and MODEM Status. The INTR signal is reset low upon the appropriate interrupt service or a Master Reset operation.

MR: Master Reset Pin 35: When this input is high, it clears all the registers (except the Receiver Buffer, Transmitter Holding, and Divisor Latches), and the control logic of the UART. The states of various output signals (SOUT, INTR, $\overline{OUT\ 1}$, $\overline{OUT\ 2}$, $\overline{RTS}$, $\overline{DTR}$) are affected by an active MR input. (Refer to Table I.) This input is buffered with a TTL-compatible Schmitt Trigger with 0.5V typical hysteresis.

$\overline{OUT\ 1}$: Output 1 Pin 34: This user-designated output can be set to an active low by programming bit 2 (OUT 1) of the MODEM Control Register to a high level. A Master Reset operation sets this signal to its inactive (high) state. Loop mode operation holds this signal in its inactive state. In the XMOS parts this will achieve TTL levels.

$\overline{OUT\ 2}$: Output 2 Pin 31: This user-designated output can be set to an active low, by programming bit 3 (OUT 2) of the MODEM Control Register to a high level. A Master Reset operation sets this signal to its inactive (high) state. Loop mode operation holds this signal in its inactive state. In the XMOS parts this will achieve TTL levels.

RCLK: Receiver Clock Pin 9: This input is the 16 × baud rate clock for the receiver section of the chip.

RD, $\overline{RD}$, Read Pins 22 and 21: When RD is high or $\overline{RD}$ is low while the chip is selected, the CPU can read status information or data from the selected UART register.

Note: Only an active RD or $\overline{RD}$ input is required to transfer data from the UART during a read operation. Therefore, tie either the RD input permanently low or the $\overline{RD}$ input permanently high, when it is not used.

$\overline{RI}$: Ring Indicator Pin 39: When low, this indicates that a telephone ringing signal has been received by the MODEM or data set. The $\overline{RI}$ signal is a MODEM status input whose condition can be tested by the CPU reading bit 6 (RI) of the MODEM Status Register. Bit 6 is the complement of the $\overline{RI}$ signal. Bit 2 (TERI) of the MODEM Status Register indicates whether the $\overline{RI}$ input **signal** has changed from a low to a high state since the previous reading of the MODEM Status Register.

Note: Whenever the RI **bit** of the MODEM Status Register changes from a high to a low state, an interrupt is generated if the MODEM Status interrupt is enabled.

$\overline{RTS}$: Request to Send Pin 32: When low, this informs the MODEM or data set that the UART is ready to exchange data. The $\overline{RTS}$ output signal can be set to an active low by programming bit 1 (RTS) of the MODEM Control Register. A Master Reset operation sets this signal to its inactive (high) state. Loop mode operation holds this signal in its inactive state.

SIN: Serial Input Pin 10: Serial data input from the communications link (peripheral device, MODEM, or data set).

SOUT: Serial Output Pin 11: This is the composite serial data output to the communications link (peripheral, MODEM or data set). The SOUT signal is set to the Marking (logic 1) state upon a Master Reset operation or when the transmitter is idle.

V_{DD}, Pin 40: +5V supply.

V_{SS}, Pin 20: Ground (0V) reference.

6.0 Pin Descriptions (Continued)

WR, $\overline{WR}$: Write Pins 19 and 18: When WR is high or $\overline{WR}$ is low while the chip is selected, the CPU can write control words or data into the selected UART register.

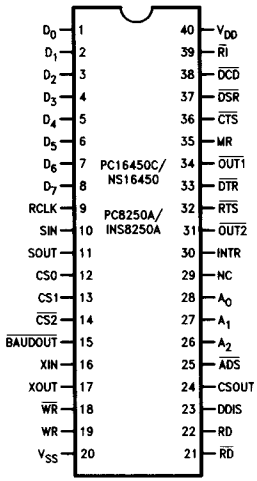
Note: Only an active WR or $\overline{WR}$ input is required to transfer data to the UART during a write operation. Therefore, tie either the WR input permanently low or the $\overline{WR}$ input permanently high, when it is not used.

XIN: (External Crystal Input), Pin 16: This signal input is used in conjunction with XOUT to form a feedback circuit for the baud rate generator's oscillator. If a clock signal will be generated off-chip, then it should drive the baud rate generator through this pin.

XOUT: (External Crystal Output), Pin 17: This signal output is used in conjunction with XIN to form a feedback circuit for the baud rate generator's oscillator. If the clock signal will be generated off-chip, then this pin is unused.

7.0 Connection Diagrams

Dual-In-Line Package

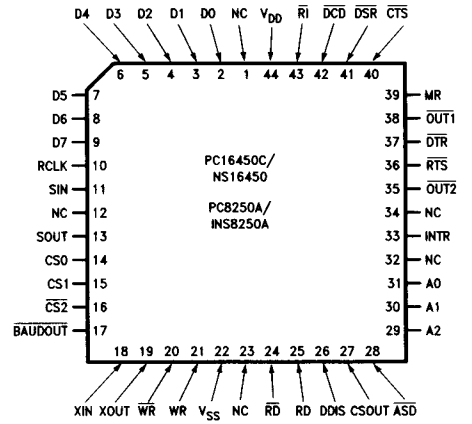


TL/C/8401-11

Top View

Order Number PC16450N/NS16450N or PC8250AN/INS8250AN See NS Package Number N40A

PLCC Package



TL/C/8401-18

Top View

Order Number PC16450V/NS16450V or PC8250AV/INS8250AV See NS Package Number V44A

TABLE I. UART Reset Functions

Register/Signal	Reset Control	Reset State
Interrupt Enable Register	Master Reset	**0000** 0000 (Note 1)
Interrupt Identification Register	Master Reset	**0000 0**001
Line Control Register	Master Reset	0000 0000
MODEM Control Register	Master Reset	**000**0 0000
Line Status Register	Master Reset	**0**110 0000
MODEM Status Register	Master Reset	XXXX 0000 (Note 2)
SOUT	Master Reset	High
INTR (RCVR Errs)	Read LSR/MR	Low
INTR (RCVR Data Ready)	Read RBR/MR	Low
INTR (THRE)	Read IIR/Write THR/MR	Low
INTR (Modem Status Changes)	Read MSR/MR	Low
$\overline{OUT\ 2}$	Master Reset	High
$\overline{RTS}$	Master Reset	High
$\overline{DTR}$	Master Reset	High
$\overline{OUT\ 1}$	Master Reset	High

Note 1: Boldface bits are permanently low.

Note 2: Bits 7–4 are driven by the input signals.

8.0 Registers

The system programmer may access any of the UART registers summarized in Table II via the CPU. These registers control UART operations including transmission and reception of data. Each register bit in Table II has its name and reset state shown.

8.1 LINE CONTROL REGISTER

The system programmer specifies the format of the asynchronous data communications exchange and sets the Divisor Latch Access bit via the Line Control Register (LCR). The programmer can also read the contents of the Line Control Register. The read capability simplifies system programming and eliminates the need for separate storage in system memory of the line characteristics. Table II shows the contents of the LCR. Details on each bit follow:

Bits 0 and 1: These two bits specify the number of bits in each transmitted or received serial character. The encoding of bits 0 and 1 is as follows:

Bit 1	Bit 0	Character Length
0	0	5 Bits
0	1	6 Bits
1	0	7 Bits
1	1	8 Bits

Bit 2: This bit specifies the number of Stop bits transmitted and received in each serial character. If bit 2 is a logic 0, one Stop bit is generated or checked in the transmitted data. If bit 2 is a logic 1 when a 5-bit word length is selected via bits 0 and 1, one and a half Stop bits are generated. If

TABLE II. Summary of Registers

	Register Address										
	0 DLAB = 0	0 DLAB = 0	1 DLAB = 0	2	3	4	5	6	7	0 DLAB = 1	1 DLAB = 1
Bit No.	Receiver Buffer Register (Read Only)	Transmitter Holding Register (Write Only)	Interrupt Enable Register	Interrupt Ident. Register (Read Only)	Line Control Register	MODEM Control Register	Line Status Register	MODEM Status Register	Scratch Register	Divisor Latch (LS)	Divisor Latch (MS)
	RBR	THR	IER	IIR	LCR	MCR	LSR	MSR	SCR	DLL	DLM
0	Data Bit 0 (Note 1)	Data Bit 0	Received Data Available	"0" if Interrupt Pending	Word Length Select Bit 0 (WLS0)	Data Terminal Ready (DTR)	Data Ready (DR)	Delta Clear to Send (DCTS)	Bit 0	Bit 0	Bit 8
1	Data Bit 1	Data Bit 1	Transmitter Holding Register Empty	Interrupt ID Bit (0)	Word Length Select Bit 1 (WLS1)	Request to Send (RTS)	Overrun Error (OE)	Delta Data Set Ready (DDSR)	Bit 1	Bit 1	Bit 9
2	Data Bit 2	Data Bit 2	Receiver Line Status	Interrupt ID Bit (1)	Number of Stop Bits (STB)	Out 1	Parity Error (PE)	Trailing Edge Ring Indicator (TERI)	Bit 2	Bit 2	Bit 10
3	Data Bit 3	Data Bit 3	MODEM Status	0	Parity Enable (PEN)	Out 2	Framing Error (FE)	Delta Data Carrier Detect (DDCD)	Bit 3	Bit 3	Bit 11
4	Data Bit 4	Data Bit 4	0	0	Even Parity Select (EPS)	Loop	Break Interrupt (BI)	Clear to Send (CTS)	Bit 4	Bit 4	Bit 12
5	Data Bit 5	Data Bit 5	0	0	Stick Parity	0	Transmitter Holding Register (THRE)	Data Set Ready (DSR)	Bit 5	Bit 5	Bit 13
6	Data Bit 6	Data Bit 6	0	0	Set Break	0	Transmitter Empty (TEMT)	Ring Indicator (RI)	Bit 6	Bit 6	Bit 14
7	Data Bit 7	Data Bit 7	0	0	Divisor Latch Access Bit (DLAB)	0	0	Data Carrier Detect (DCD)	Bit 7	Bit 7	Bit 15

Note 1: Bit 0 is the least significant bit. It is the first bit serially transmitted or received.

8.0 Registers (Continued)

bit 2 is a logic 1 when either a 6-, 7-, or 8-bit word length is selected, two Stop bits are generated. The Receiver checks the first Stop-bit only, regardless of the number of Stop bits selected.

Bit 3: This bit is the Parity Enable bit. When bit 3 is a logic 1, a Parity bit is generated (transmit data) or checked (receive data) between the last data word bit and Stop bit of the serial data. (The Parity bit is used to produce an even or odd number of 1s when the data word bits and the Parity bit are summed.)

Bit 4: This bit is the Even Parity Select bit. When bit 3 is a logic 1 and bit 4 is a logic 0, an odd number of logic 1s is transmitted or checked in the data word bits and Parity bit. When bit 3 is a logic 1 and bit 4 is a logic 1, an even number of logic 1s is transmitted or checked.

Bit 5: This bit is the Stick Parity bit. When bits 3, 4 and 5 are logic 1 the Parity bit is transmitted and checked as a logic 0. If bits 3 and 5 are 1 and bit 4 is a logic 0 then the Parity bit is transmitted and checked as a logic 1. If bit 5 is a logic 0 Stick Parity is disabled.

Bit 6: This bit is the Break Control bit. It causes a break condition to be transmitted by the UART. When it is set to a logic 1, the serial output (SOUT) is forced to the Spacing (logic 0) state. The break is disabled by clearing bit 6 to a logic 0. The Break Control bit acts only on SOUT and has no effect on the transmitter logic.

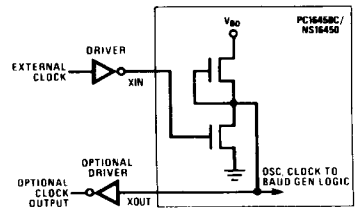
Note: This feature enables the CPU to alert a terminal in a computer communications system. If the following sequence is used, no erroneous or extraneous characters will be transmitted because of the break.

1. Load an all 0s, pad character, in response to THRE.
2. Set break after the next THRE.
3. Wait for the transmitter to be idle, (TEMT = 1), and clear break when normal transmission has to be restored.

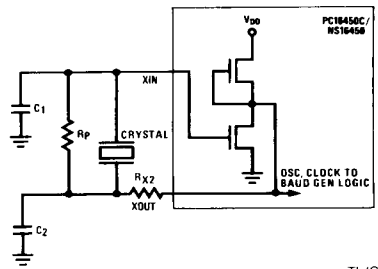
During the break, the Transmitter can be used as a character timer to accurately establish the break duration.

Bit 7: This bit is the Divisor Latch Access Bit (DLAB). It must be set high (logic 1) to access the Divisor Latches of the Baud Generator during a Read or Write operation. It must be set low (logic 0) to access the Receiver Buffer, the Transmitter Holding Register, or the Interrupt Enable Register.

8.2 TYPICAL CLOCK CIRCUITS



TL/C/8401–12



TL/C/8401–13

Typical Oscillator Networks

Crystal	R_P	R_{X2}	C_1	C_2
1.8–8 MHz	1 MΩ	1.5k	10–30 pF	40–60 pF

Note: These R and C values are approximate and may vary 2X depending on the crystal characteristics. All crystal circuits should be designed specifically for the system.

TABLE III. Baud Rates, Divisors and Crystals

Baud Rate	1.8432 MHz Crystal		3.072 MHz Crystal		8.0 MHz Crystal	
	Decimal Divisor for 16 × Clock	Percent Error	Decimal Divisor for 16 × Clock	Percent Error	Decimal Divisor for 16 × Clock	Percent Error
50	2304	—	3840	—	10000	—
75	1536	—	2560	—	6667	0.005
110	1047	0.026	1745	0.026	4545	0.010
134.5	857	0.058	1428	0.034	3717	0.013
150	768	—	1280	—	3333	0.010
300	384	—	640	—	1667	0.020
600	192	—	320	—	833	0.040
1200	96	—	160	—	417	0.080
1800	64	—	107	0.312	277	0.080
2000	58	0.69	96	—	250	—
2400	48	—	80	—	208	0.160
3600	32	—	53	0.628	139	0.080
4800	24	—	40	—	104	0.160
7200	16	—	27	1.23	69	0.644
9600	12	—	20	—	52	0.160
19200	6	—	10	—	26	0.160
38400	3	—	5	—	13	0.160
56000	2	2.86	—	—	9	0.790
128000	—	—	—	—	4	2.344
					2	2.344

8.0 Registers (Continued)

8.3 PROGRAMMABLE BAUD GENERATOR

The UART contains a programmable Baud Generator that is capable of taking any clock input from DC to 8 MHz and dividing it by any divisor from 1 to $2^{16}-1$. The output frequency of the Baud Generator is 16 × the Baud [divisor # = (frequency input) ÷ (baud rate × 16)]. Two 8-bit latches store the divisor in a 16-bit binary format. These Divisor Latches must be loaded during initialization in order to ensure proper operation of the Baud Generator. Upon loading either of the Divisor Latches, a 16-bit Baud counter is immediately loaded.

Table III provides decimal divisors to use with crystal frequencies of 1.8432 MHz, 3.072 MHz and 8 MHz for common baud rates. For baud rates of 38400 and below, the error obtained is minimal. The accuracy of the desired baud rate is dependent on the crystal frequency chosen. Using a division of 0 is **not** recommended.

8.4 LINE STATUS REGISTER

This 8-bit register provides status information to the CPU concerning the data transfer. Table II shows the contents of the Line Status Register. Details on each bit follow:

Bit 0: This bit is the receiver Data Ready (DR) indicator. Bit 0 is set to a logic 1 whenever a complete incoming character has been received and transferred into the Receiver Buffer Register. Bit 0 is reset to a logic 0 by reading the data in the Receiver Buffer Register.

Bit 1: This bit is the Overrun Error (OE) indicator. Bit 1 indicates that data in the Receiver Buffer Register was not read by the CPU before the next character was transferred into the Receiver Buffer Register, thereby destroying the previous character. The OE indicator is set to a logic 1 upon detection of an overrun condition and reset whenever the CPU reads the contents of the Line Status Register.

Bit 2: This bit is the Parity Error (PE) indicator. Bit 2 indicates that the received data character does not have the correct even or odd parity, as selected by the even-parity-select bit. The PE bit is set to a logic 1 upon detection of a parity error and is reset to a logic 0 whenever the CPU reads the contents of the Line Status Register.

Bit 3: This bit is the Framing Error (FE) indicator. Bit 3 indicates that the received character did not have a valid Stop bit. Bit 3 is set to a logic 1 whenever the Stop bit following the last data bit or parity bit is a logic 0 (Spacing level). The FE indicator is reset whenever the CPU reads the contents of the Line Status Register. The UART will try to resynchronize after a framing error. To do this it assumes that the framing error was due to the next start bit, so it samples this "start" bit twice and then takes in the "data".

Bit 4: This bit is the Break Interrupt (BI) indicator. Bit 4 is set to a logic 1 whenever the received data input is held in the Spacing (logic 0) state for longer than a full word transmission time (that is, the total time of Start bit + data bits + Parity + Stop bits). The BI indicator is reset whenever the CPU reads the contents of the Line Status Register. Restarting after a break is received, requires the SIN pin to be logical 1 for at least ½ bit time.

Note: Bits 1 through 4 are the error conditions that produce a Receiver Line Status interrupt whenever any of the corresponding conditions are detected and the interrupt is enabled.

Bit 5: This bit is the Transmitter Holding Register Empty (THRE) indicator. Bit 5 indicates that the UART is ready to accept a new character for transmission. In addition, this bit causes the UART to issue an interrupt to the CPU when the Transmit Holding Register Empty Interrupt enable is set high. The THRE bit is set to a logic 1 when a character is transferred from the Transmitter Holding Register into the Transmitter Shift Register. The bit is reset to logic 0 whenever the CPU loads the Transmitter Holding Register.

Bit 6: This bit is the Transmitter Empty (TEMT) indicator. Bit 6 is set to a logic 1 whenever the Transmitter Holding Register (THR) and the Transmitter Shift Register (TSR) are both empty. It is reset to a logic 0 whenever either the THR or TSR contains a data character.

Bit 7: This bit is permanently set to logic 0.

Note: The Line Status Register is intended for read operations only. Writing to this register is not recommended as this operation is only used for factory testing.

TABLE IV. Interrupt Control Functions

Interrupt Identification Register				Interrupt Set and Reset Functions		
Bit 2	Bit 1	Bit 0	Priority Level	Interrupt Type	Interrupt Source	Interrupt Reset Control
0	0	1	—	None	None	—
1	1	0	Highest	Receiver Line Status	Overrun Error or Parity Error or Framing Error or Break Interrupt	Reading the Line Status Register
1	0	0	Second	Received Data Available	Receiver Data Available	Reading the Receiver Buffer Register
0	1	0	Third	Transmitter Holding Register Empty	Transmitter Holding Register Empty	Reading the IIR Register (if source of interrupt) or Writing into the Transmitter Holding Register
0	0	0	Fourth	MODEM Status	Clear to Send or Data Set Ready or Ring Indicator or Data Carrier Detect	Reading the MODEM Status Register

8.0 Registers (Continued)

8.5 INTERRUPT IDENTIFICATION REGISTER

In order to provide minimum software overhead during data character transfers, the UART prioritizes interrupts into four levels and records these in the Interrupt Identification Register. The four levels of interrupt conditions in order of priority are Receiver Line Status; Received Data Ready; Transmitter Holding Register Empty; and MODEM Status.

When the CPU accesses the IIR, the UART freezes all interrupts and indicates the highest priority pending interrupt to the CPU. While this CPU access is occurring, the UART records new interrupts, but does not change its current indication until the access is complete. Table II shows the contents of the IIR. Details on each bit follow:

Bit 0: This bit can be used in an interrupt environment to indicate whether an interrupt condition is pending. When bit 0 is a logic 0, an interrupt is pending and the IIR contents may be used as a pointer to the appropriate interrupt service routine. When bit 0 is a logic 1, no interrupt is pending.

Bits 1 and 2: These two bits of the IIR are used to identify the highest priority interrupt pending as indicated in Table IV.

Bits 3 through 7: These five bits of the IIR are always logic 0.

8.6 INTERRUPT ENABLE REGISTER

This register enables the four types of UART interrupts. Each interrupt can individually activate the interrupt (INTR) output signal. It is possible to totally disable the interrupt system by resetting bits 0 through 3 of the Interrupt Enable Register (IER). Similarly, setting bits of this register to a logic 1, enables the selected interrupt(s). Disabling an interrupt prevents it from being indicated as active in the IIR and from activating the INTR output signal. All other system functions operate in their normal manner, including the setting of the Line Status and MODEM Status Registers. Table II shows the contents of the IER. Details on each bit follow.

Bit 0: This bit enables the Received Data Available Interrupt when set to logic 1.

Bit 1: This bit enables the Transmitter Holding Register Empty Interrupt when set to logic 1.

Bit 2: This bit enables the Receiver Line Status Interrupt when set to logic 1.

Bit 3: This bit enables the MODEM Status Interrupt when set to logic 1.

Bits 4 through 7: These four bits are always logic 0.

8.7 MODEM CONTROL REGISTER

This register controls the interface with the MODEM or data set (or a peripheral device emulating a MODEM). The contents of the MODEM Control Register (MCR) are indicated in Table II and are described below. Table II shows the contents of the MCR. Details on each bit follow.

Bit 0: This bit controls the Data Terminal Ready ($\overline{DTR}$) output. When bit 0 is set to a logic 1, the $\overline{DTR}$ output is forced to a logic 0. When bit 0 is reset to a logic 0, the $\overline{DTR}$ output is forced to a logic 1.

Note: The $\overline{DTR}$ output of the UART may be applied to an EIA inverting line driver (such as the DS1488) to obtain the proper polarity input at the succeeding MODEM or data set.

Bit 1: This bit controls the Request to Send ($\overline{RTS}$) output. Bit 1 affects the $\overline{RTS}$ output in a manner identical to that described above for bit 0.

Bit 2: This bit controls the Output 1 ($\overline{OUT\ 1}$) signal, which is an auxiliary user-designated output. Bit 2 affects the $\overline{OUT\ 1}$ output in a manner identical to that described above for bit 0.

Bit 3: This bit controls the Output 2 ($\overline{OUT\ 2}$) signal, which is an auxiliary user-designated output. Bit 3 affects the $\overline{OUT\ 2}$ output in a manner identical to that described above for bit 0.

Bit 4: This bit provides a local loopback feature for diagnostic testing of the UART. When bit 4 is set to logic 1, the following occur: the transmitter Serial Output (SOUT) is set to the Marking (logic 1) state; the receiver Serial Input (SIN) is disconnected; the output of the Transmitter Shift Register is "looped back" into the Receiver Shift Register input; the four MODEM Control inputs ($\overline{DSR}$, $\overline{CTS}$, $\overline{RI}$, and $\overline{DCD}$) are disconnected; and the four MODEM Control outputs ($\overline{DTR}$, $\overline{RTS}$, $\overline{OUT\ 1}$, and $\overline{OUT\ 2}$) are internally connected to the four MODEM Control inputs. The MODEM Control output pins are forced to their inactive state (high). In the loopback mode, data that is transmitted is immediately received. This feature allows the processor to verify the transmit-and received-data paths of the UART.

In the loopback mode, the receiver and transmitter interrupts are fully operational. The MODEM Control Interrupts are also operational, but the interrupts' sources are now the lower four bits of the MODEM Control Register instead of the four MODEM Control inputs. The interrupts are still controlled by the Interrupt Enable Register.

Bits 5 through 7: These bits are permanently set to logic 0.

8.8 MODEM STATUS REGISTER

This register provides the current state of the control lines from the MODEM (or peripheral device) to the CPU. In addition to this current-state information, four bits of the MODEM Status Register provide change information. These bits are set to a logic 1 whenever a control input from the MODEM changes state. They are reset to logic 0 whenever the CPU reads the MODEM Status Register.

8.0 Registers (Continued)

Table II shows the contents of the MSR. Details on each bit follow.

Bit 0: This bit is the Delta Clear to Send (DCTS) indicator. Bit 0 indicates that the $\overline{CTS}$ input to the chip has changed state since the last time it was read by the CPU.

Bit 1: This bit is the Delta Data Set Ready (DDSR) indicator. Bit 1 indicates that the $\overline{DSR}$ input to the chip has changed state since the last time it was read by the CPU.

Bit 2: This bit is the Trailing Edge of Ring Indicator (TERI) detector. Bit 2 indicates that the $\overline{RI}$ input to the chip has changed from a low to a high state.

Bit 3: This bit is the Delta Data Carrier Detect (DDCD) indicator. Bit 3 indicates that the $\overline{DCD}$ input to the chip has changed state.

Note: Whenever bit 0, 1, 2, or 3 is set to logic 1, a MODEM Status Interrupt is generated.

Bit 4: This bit is the complement of the Clear to Send ($\overline{CTS}$) input. If bit 4 (loop) of the MCR is set to a 1, this bit is equivalent to RTS in the MCR.

Bit 5: This bit is the complement of the Data Set Ready ($\overline{DSR}$) input. If bit 4 of the MCR is set to a 1, this bit is equivalent to DTR in the MCR.

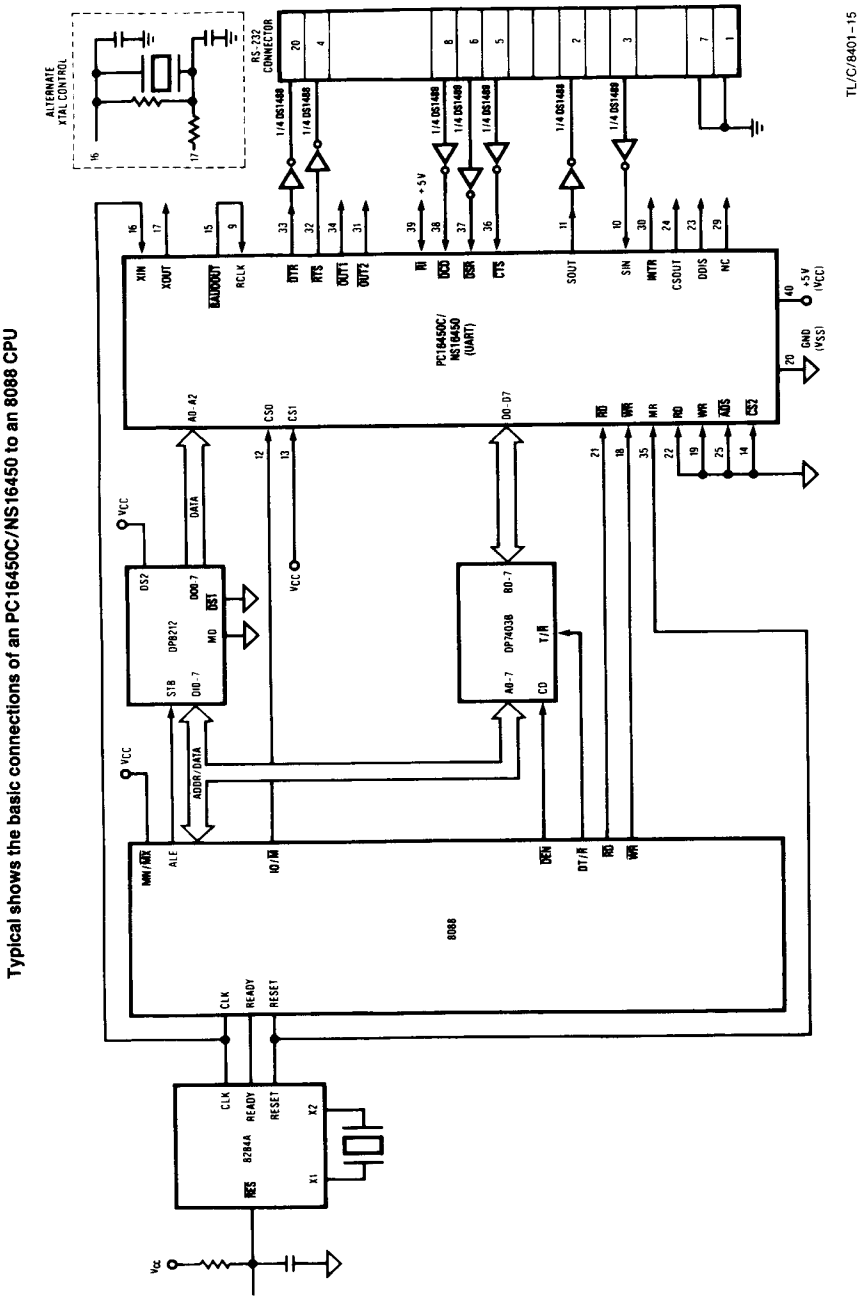
Bit 6: This bit is the complement of the Ring Indicator ($\overline{RI}$) input. If bit 4 of the MCR is set to a 1, this bit is equivalent to OUT 1 in the MCR.

Bit 7: This bit is the complement of the Data Carrier Detect ($\overline{DCD}$) input. If bit 4 of the MCR is set to a 1, this bit is equivalent to OUT 2 in the MCR.

8.9 SCRATCHPAD REGISTER

This 8-bit Read/Write Register does not control the UART in any way. It is intended as a scratchpad register to be used by the programmer to hold data temporarily.

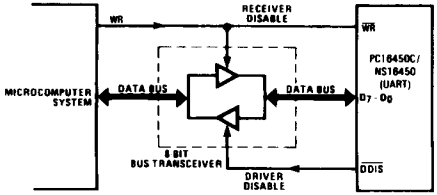
9.0 Typical Applications



Typical shows the basic connections of an PC16450C/NS16450 to an 8088 CPU

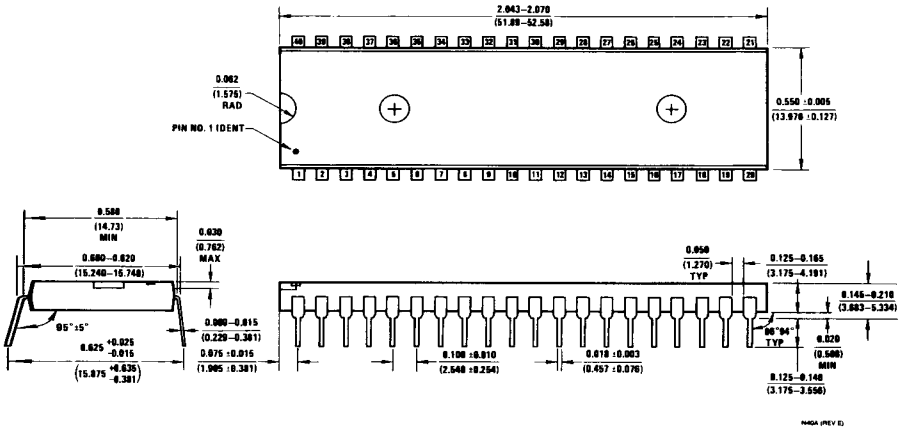
9.0 Typical Applications (Continued)

Typical Interface for a High-Capacity Data Bus



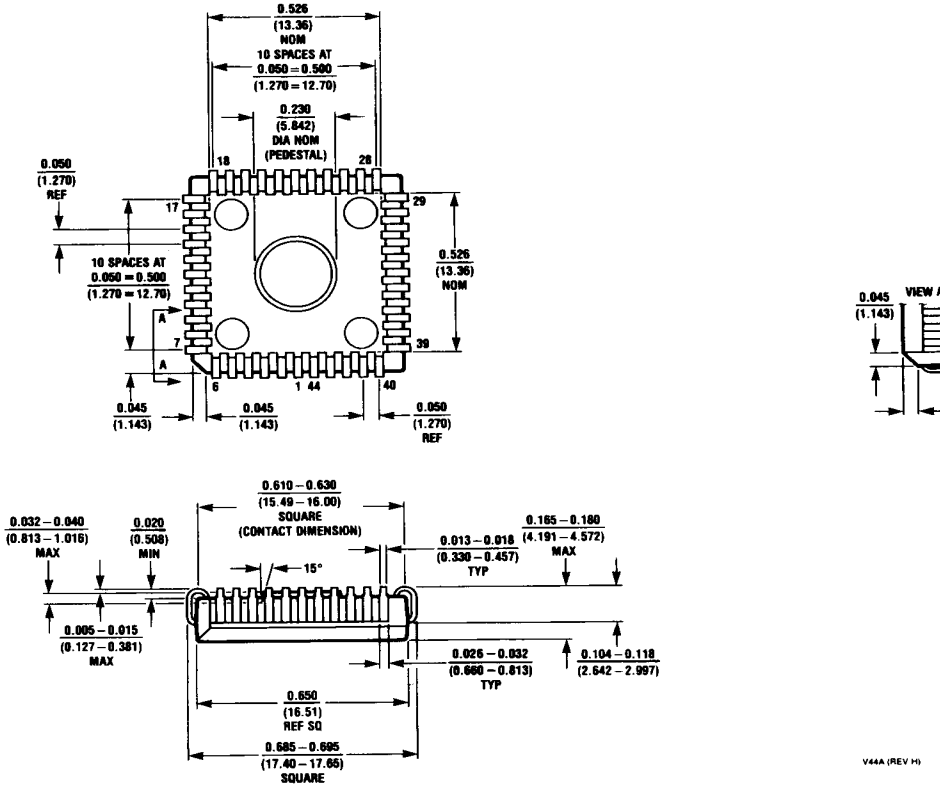
TL/C/8401–16

Physical Dimensions inches (millimeters)



Plastic Dual-In-Line Package (N)
Order Number PC16450N/NS16450N or PC8250AN/INS8250AN
NS Package Number N40A

Physical Dimensions inches (millimeters) (Continued)



44-Lead Plastic Chip Carrier (V)
Order Number PC16450V/NS16450V or PC8250AV/INS8250AV
NS Package Number V44A

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2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

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MOTOROLA

MC6821

PERIPHERAL INTERFACE ADAPTER (PIA)

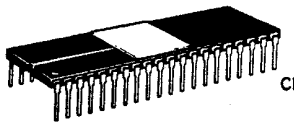
The MC6821 Peripheral Interface Adapter provides the universal means of interfacing peripheral equipment to the M6800 family of microprocessors. This device is capable of interfacing the MPU to peripherals through two 8-bit bidirectional peripheral data buses and four control lines. No external logic is required for interfacing to most peripheral devices.

The functional configuration of the PIA is programmed by the MPU during system initialization. Each of the peripheral data lines can be programmed to act as an input or output, and each of the four control/interrupt lines may be programmed for one of several control modes. This allows a high degree of flexibility in the overall operation of the interface.

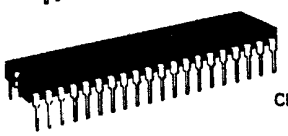
- 8-Bit Bidirectional Data Bus for Communication with the MPU
- Two Bidirectional 8-Bit Buses for Interface to Peripherals
- Two Programmable Control Registers
- Two Programmable Data Direction Registers
- Four Individually-Controlled Interrupt Input Lines; Two Usable as Peripheral Control Outputs
- Handshake Control Logic for Input and Output Peripheral Operation
- High-Impedance Three-State and Direct Transistor Drive Peripheral Lines
- Program Controlled Interrupt and Interrupt Disable Capability
- CMOS Drive Capability on Side A Peripheral Lines
- Two TTL Drive Capability on All A and B Side Buffers
- TTL-Compatible
- Static Operation

MOS
(N-CHANNEL, SILICON-GATE, DEPLETION LOAD)

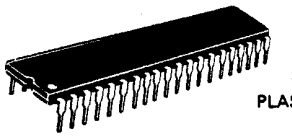
PERIPHERAL INTERFACE ADAPTER



L SUFFIX
CERAMIC PACKAGE
CASE 715



S SUFFIX
CERDIP PACKAGE
CASE 734



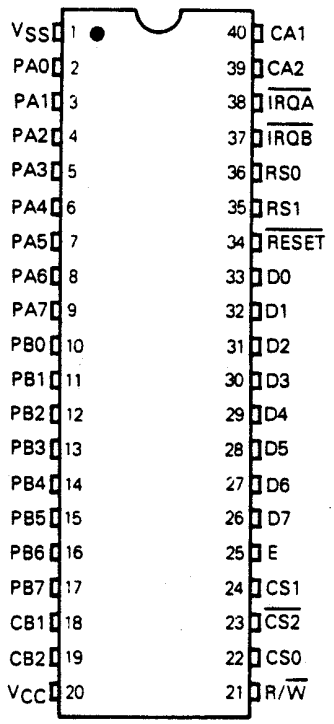
P SUFFIX
PLASTIC PACKAGE
CASE 711

3

ORDERING INFORMATION

Package Type	Frequency (MHz)	Temperature	Order Number
Ceramic L Suffix	1.0	0°C to 70°C	MC6821L
	1.0	−40°C to 85°C	MC6821CL
	1.5	0°C to 70°C	MC68A21L
	1.5	−40°C to 85°C	MC68A21CL
	2.0	0°C to 70°C	MC68B21L
Cerdip S Suffix	1.0	0°C to 70°C	MC6821S
	1.0	−40°C to 85°C	MC6821CS
	1.5	0°C to 70°C	MC68A21S
	1.5	−40°C to 85°C	MC68A21CS
	2.0	0°C to 70°C	MC68B21S
Plastic P Suffix	1.0	0°C to 70°C	MC6821P
	1.0	−40°C to 85°C	MC6821CP
	1.5	0°C to 70°C	MC68A21P
	1.5	−40°C to 85°C	MC68A21CP
	2.0	0°C to 70°C	MC68B21P

PIN ASSIGNMENT



MAXIMUM RATINGS

Characteristics	Symbol	Value	Unit
Supply Voltage	V_{CC}	−0.3 to +7.0	V
Input Voltage	V_{in}	−0.3 to +7.0	V
Operating Temperature Range MC6821, MC68A21, MC68B21 MC6821C, MC68A21C	T_A	T_L to T_H 0 to 70 −40 to +85	°C
Storage Temperature Range	T_{stg}	−55 to +150	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Value	Unit
Thermal Resistance Ceramic Plastic Cerdip	θ_{JA}	 50 100 60	°C/W

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $GND \leq (V_{in}$ or $V_{out}) \leq V_{CC}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}).

3

POWER CONSIDERATIONS

The average chip-junction temperature, T_J, in °C can be obtained from:

$$T_J = T_A + (P_D \bullet \theta_{JA}) \quad (1)$$

Where:

T_A ≡ Ambient Temperature, °C

θ_{JA} ≡ Package Thermal Resistance, Junction-to-Ambient, °C/W

$P_D \equiv P_{INT} + P_{PORT}$

$P_{INT} \equiv I_{CC} \times V_{CC}$, Watts — Chip Internal Power

P_{PORT} ≡ Port Power Dissipation, Watts — User Determined

For most applications $P_{PORT} \ll P_{INT}$ and can be neglected. P_{PORT} may become significant if the device is configured to drive Darlington bases or sink LED loads.

An approximate relationship between P_D and T_J (if P_{PORT} is neglected) is:

$$P_D = K \div (T_J + 273°C) \quad (2)$$

Solving equations 1 and 2 for K gives:

$$K = P_D \bullet (T_A + 273°C) + \theta_{JA} \bullet P_D^2 \quad (3)$$

Where K is a constant pertaining to the particular part. K can be determined from equation 3 by measuring P_D (at equilibrium) for a known T_A. Using this value of K the values of P_D and T_J can be obtained by solving equations (1) and (2) iteratively for any value of T_A.

DC ELECTRICAL CHARACTERISTICS (V_{CC} = 5.0 Vdc ±5%, V_{SS} = 0, $T_A = T_L$ to T_H unless otherwise noted).

Characteristic	Symbol	Min	Typ	Max	Unit
BUS CONTROL INPUTS (R/$\overline{W}$, Enable, $\overline{RESET}$, RS0, RS1, CS0, CS1, CS2)					
Input High Voltage	V_{IH}	V_{SS}+2.0	–	V_{CC}	V
Input Low Voltage	V_{IL}	V_{SS}−0.3	–	V_{SS}+0.8	V
Input Leakage Current (V_{in} = 0 to 5.25 V)	I_{in}	–	1.0	2.5	μA
Capacitance (V_{in} = 0, T_A = 25°C, f = 1.0 MHz)	C_{in}	–	–	7.5	pF
INTERRUPT OUTPUTS ($\overline{IRQA}$, $\overline{IRQB}$)					
Output Low Voltage (I_{Load} = 1.6 mA)	V_{OL}	–	–	V_{SS}+0.4	V
Hi-Z Output Leakage Current	I_{OZ}	–	1.0	10	μA
Capacitance (V_{in} = 0, T_A = 25°C, f = 1.0 MHz)	C_{out}	–	–	5.0	pF
DATA BUS (D0-D7)					
Input High Voltage	V_{IH}	V_{SS}+2.0	–	V_{CC}	V
Input Low Voltage	V_{IL}	V_{SS}−0.3	–	V_{SS}+0.8	V
Hi-Z Input Leakage Current (V_{in} = 0.4 to 2.4 V)	I_{IZ}	–	2.0	10	μA
Output High Voltage (I_{Load} = −205 μA)	V_{OH}	V_{SS}+2.4	–	–	V
Output Low Voltage (I_{Load} = 1.6 mA)	V_{OL}	–	–	V_{SS}+0.4	V
Capacitance (V_{in} = 0, T_A = 25°C, f = 1.0 MHz)	C_{in}	–	–	12.5	pF

DC ELECTRICAL CHARACTERISTICS (Continued)

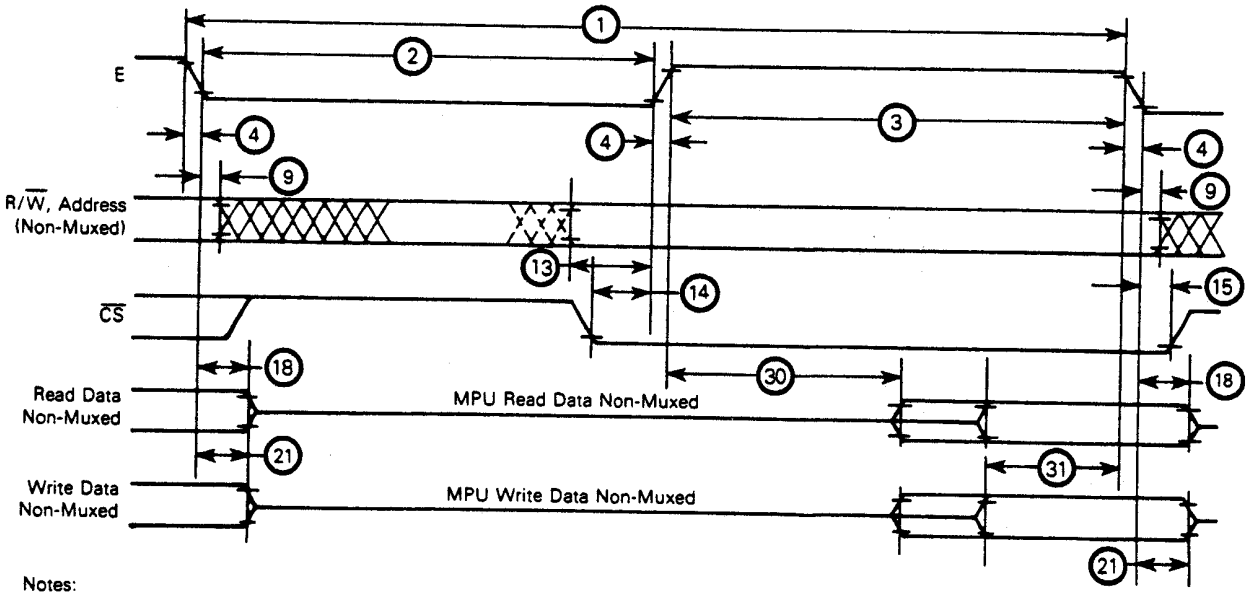
Characteristic		Symbol	Min	Typ	Max	Unit
PERIPHERAL BUS (PA0-PA7, PB0-PB7, CA1, CA2, CB1, CB2)						
Input Leakage Current (V_{in} = 0 to 5.25 V)	R/$\overline{W}$, $\overline{RESET}$, RS0, RS1, CS0, CS1, $\overline{CS2}$, CA1, CB1, Enable	I_{in}	–	1.0	2.5	μA
Hi-Z Input Leakage Current (V_{in} = 0.4 to 2.4 V)	PB0-PB7, CB2	I_{IZ}	–	2.0	10	μA
Input High Current (V_{IH} = 2.4 V)	PA0-PA7, CA2	I_{IH}	–200	–400	–	μA
Darlington Drive Current (V_O = 1.5 V)	PB0-PB7, CB2	I_{OH}	–1.0	–	–10	mA
Input Low Current (V_{IL} = 0.4 V)	PA0-PA7, CA2	I_{IL}	–	–1.3	–2.4	mA
Output High Voltage (I_{Load} = –200 μA)	PA0-PA7, PB0-PB7, CA2, CB2	V_{OH}	V_{SS} + 2.4	–	–	V
(I_{Load} = –10 μA)	PA0-PA7, CA2		V_{CC} – 1.0	–	–	
Output Low Voltage (I_{Load} = 3.2 mA)		V_{OL}	–	–	V_{SS} + 0.4	V
Capacitance (V_{in} = 0, T_A = 25°C, f = 1.0 MHz)		C_{in}	–	–	10	pF
POWER REQUIREMENTS						
Internal Power Dissipation (Measured at T_L = 0°C)		P_{INT}	–	–	550	mW

BUS TIMING CHARACTERISTICS (See Notes 1 and 2)

Ident. Number	Characteristic	Symbol	MC6821		MC68A21		MC68B21		Unit
			Min	Max	Min	Max	Min	Max	
1	Cycle Time	t_{cyc}	1.0	10	0.67	10	0.5	10	μs
2	Pulse Width, E Low	PW_{EL}	430	–	280	–	210	–	ns
3	Pulse Width, E High	PW_{EH}	450	–	280	–	220	–	ns
4	Clock Rise and Fall Time	t_r, t_f	–	25	–	25	–	20	ns
9	Address Hold Time	t_{AH}	10	–	10	–	10	–	ns
13	Address Setup Time Before E	t_{AS}	80	–	60	–	40	–	ns
14	Chip Select Setup Time Before E	t_{CS}	80	–	60	–	40	–	ns
15	Chip Select Hold Time	t_{CH}	10	–	10	–	10	–	ns
18	Read Data Hold Time	t_{DHR}	20	50*	20	50*	20	50*	ns
21	Write Data Hold Time	t_{DHW}	10	–	10	–	10	–	ns
30	Output Data Delay Time	t_{DDR}	–	290	–	180	–	150	ns
31	Input Data Setup Time	t_{DSW}	165	–	80	–	60	–	ns

*The data bus output buffers are no longer sourcing or sinking current by t_{DHR}max (High Impedance).

FIGURE 1 — BUS TIMING



Notes:
1. Voltage levels shown are $V_L \leq 0.4$ V, $V_H \geq 2.4$ V, unless otherwise specified.
2. Measurement points shown are 0.8 V and 2.0 V, unless otherwise specified.

PERIPHERAL TIMING CHARACTERISTICS (V_{CC} = 5.0 V ±5%, V_{SS} = 0 V, $T_A = T_L$ to T_H unless otherwise specified)

Characteristic	Symbol	MC6821		MC68A21		MC68B21		Unit	Reference Fig. No.
		Min	Max	Min	Max	Min	Max		
Data Setup Time	t_{PDS}	200	–	135	–	100	–	ns	6
Data Hold Time	t_{PDH}	0	–	0	–	0	–	ns	6
Delay Time, Enable Negative Transition to CA2 Negative Transition	t_{CA2}	–	1.0	–	0.670	–	0.500	µs	3, 7, 8
Delay Time, Enable Negative Transition to CA2 Positive Transition	T_{RS1}	–	1.0	–	0.670	–	0.500	µs	3, 7
Rise and Fall Times for CA1 and CA2 Input Signals	t_r, t_f	–	1.0	–	1.0	–	1.0	µs	8
Delay Time from CA1 Active Transition to CA2 Positive Transition	t_{RS2}	–	2.0	–	1.35	–	1.0	µs	3, 8
Delay Time, Enable Negative Transition to Data Valid	t_{PDW}	–	1.0	–	0.670	–	0.5	µs	3, 9, 10
Delay Time, Enable Negative Transition to CMOS Data Valid PA0-PA7, CA2	t_{CMOS}	–	2.0	–	1.35	–	1.0	µs	4, 9
Delay Time, Enable Positive Transition to CB2 Negative Transition	t_{CB2}	–	1.0	–	0.670	–	0.5	µs	3, 11, 12
Delay Time, Data Valid to CB2 Negative Transition	t_{DC}	20	–	20	–	20	–	ns	3, 10
Delay Time, Enable Positive Transition to CB2 Positive Transition	t_{RS1}	–	1.0	–	0.670	–	0.5	µs	3, 11
Control Output Pulse Width, CA2/CB2	PW_{CT}	500	–	375	–	250	–	ns	3, 11
Rise and Fall Time for CB1 and CB2 Input Signals	t_r, t_f	–	1.0	–	1.0	–	1.0	µ	12
Delay Time, CB1 Active Transition to CB2 Positive Transition	t_{RS2}	–	2.0	–	1.35	–	1.0	µs	3, 12
Interrupt Release Time, $\overline{IRQA}$ and $\overline{IRQB}$	t_{IR}	–	1.60	–	1.10	–	0.85	µs	5, 14
Interrupt Response Time	t_{RS3}	–	1.0	–	1.0	–	1.0	µs	5, 13
Interrupt Input Pulse Time	PW_I	500	–	500	–	500	–	ns	13
$\overline{RESET}$ Low Time*	t_{RL}	1.0	–	0.66	–	0.5	–	µs	15

*The $\overline{RESET}$ line must be high a minimum of 1.0 µs before addressing the PIA.

FIGURE 2 – BUS TIMING TEST LOADS

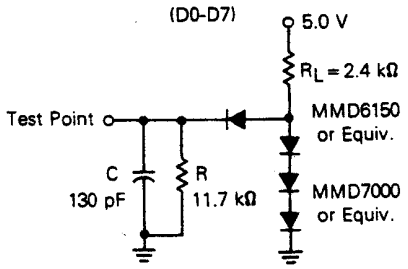


FIGURE 3 – TTL EQUIVALENT TEST LOAD

(PA0–PA7, PB0–PB7, CA2, CB2)

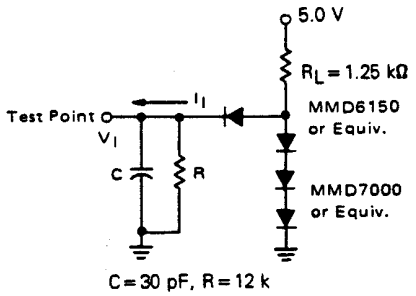


FIGURE 4 – CMOS EQUIVALENT TEST LOAD

(PA0-PA7, CA2)

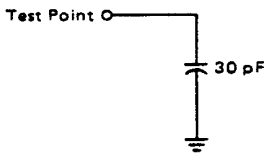


FIGURE 5 – NMOS EQUIVALENT TEST LOAD

($\overline{IRQ}$ Only)

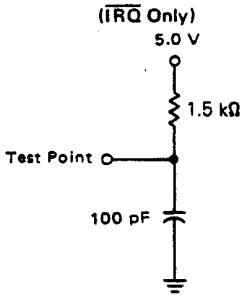


FIGURE 6 — PERIPHERAL DATA SETUP AND HOLD TIMES
(Read Mode)

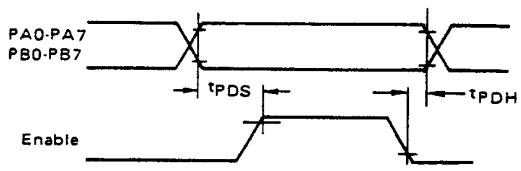
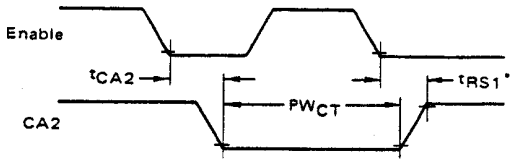


FIGURE 7 — CA2 DELAY TIME
(Read Mode; CRA-5 = CRA3 = 1, CRA-4 = 0)



*Assumes part was deselected during the previous E pulse.

FIGURE 8 — CA2 DELAY TIME
(Read Mode; CRA-5 = 1, CRA-3 = CRA-4 = 0)

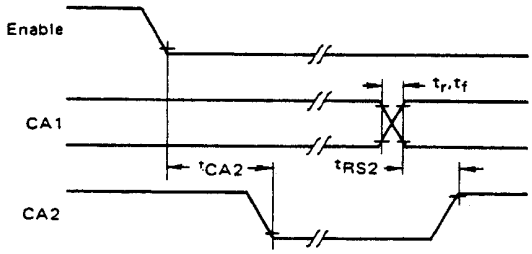


FIGURE 9 — PERIPHERAL CMOS DATA DELAY TIMES
(Write Mode; CRA-5 = CRA-3 = 1, CRA-4 = 0)

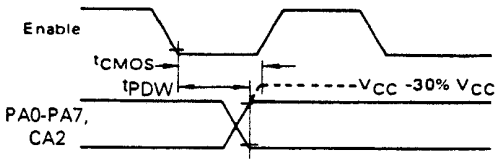
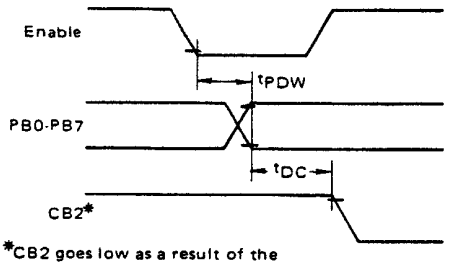
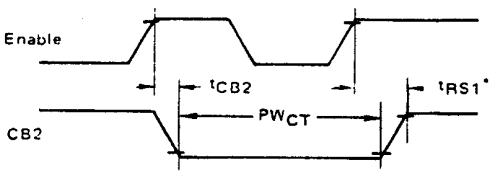


FIGURE 10 — PERIPHERAL DATA AND CB2 DELAY TIMES
(Write Mode; CRB-5 = CRB-3 = 1, CRB-4 = 0)



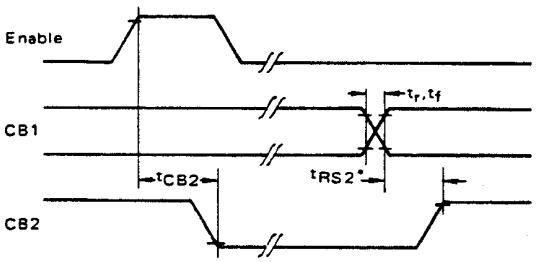
*CB2 goes low as a result of the positive transition of Enable.

FIGURE 11 — CB2 DELAY TIME
(Write Mode; CRB-5 = CRB-3 = 1, CRB-4 = 0)



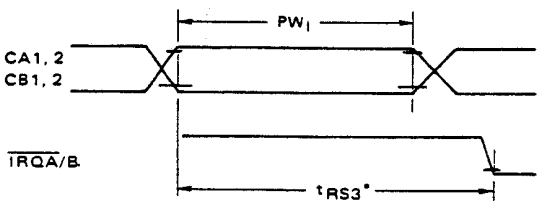
*Assumes part was deselected during the previous E pulse.

FIGURE 12 — CB2 DELAY TIME
(Write Mode; CRB-5 = 1, CRB-3 = CRB-4 = 0)



*Assumes part was deselected during any previous E pulse.

FIGURE 13 — INTERRUPT PULSE WIDTH AND $\overline{IRQ}$ RESPONSE



*Assumes Interrupt Enable Bits are set.

Note: Timing measurements are referenced to and from a low voltage of 0.8 volts and a high voltage of 2.0 volts, unless otherwise noted.

FIGURE 14 — $\overline{IRQ}$ RELEASE TIME

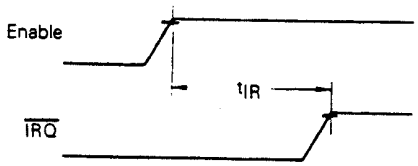
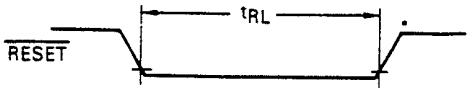


FIGURE 15 — $\overline{RESET}$ LOW TIME

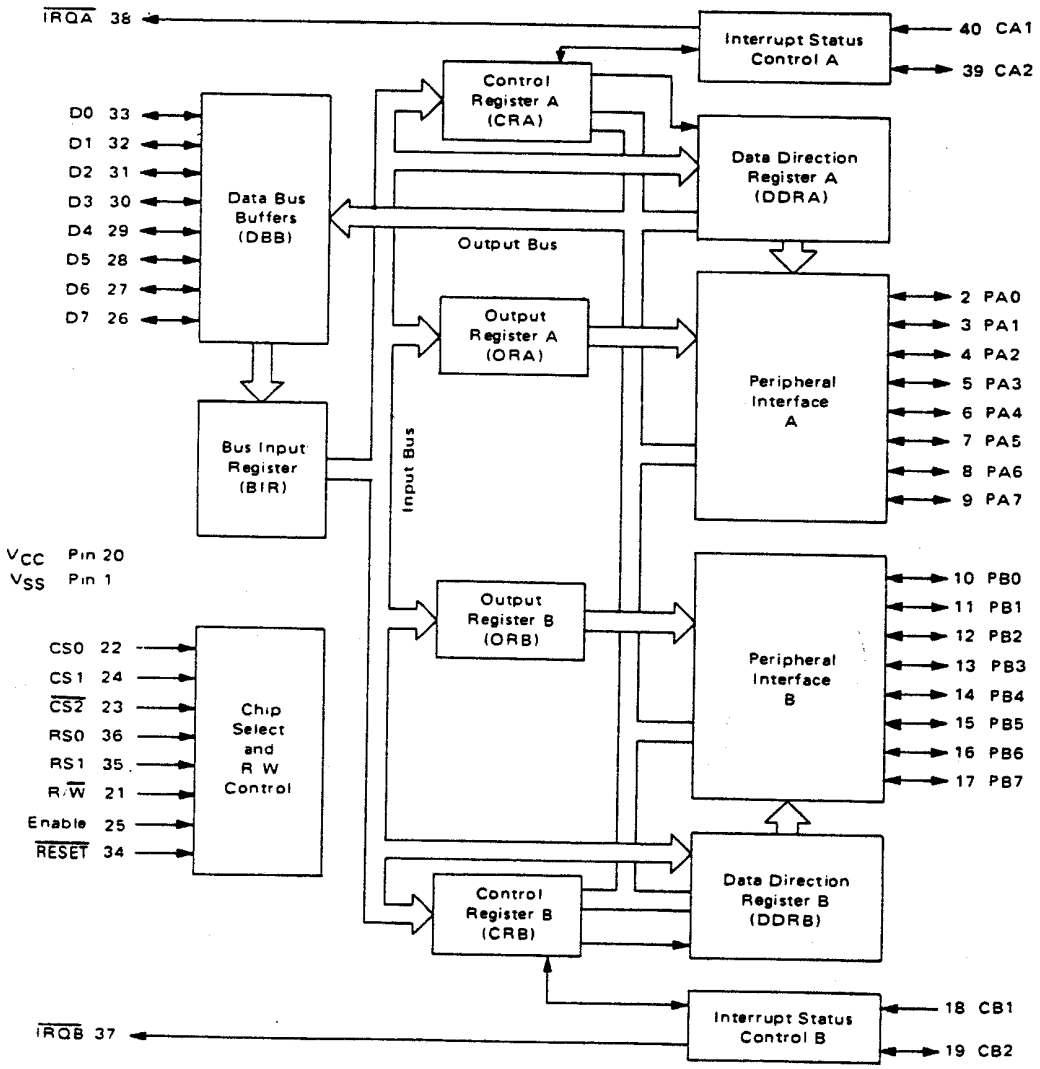


*The $\overline{RESET}$ line must be a V_{IH} for a minimum of 1.0 μs before addressing the PIA.

Note: Timing measurements are referenced to and from a low voltage of 0.8 volts and a high voltage of 2.0 volts, unless otherwise noted.

3

FIGURE 16 — EXPANDED BLOCK DIAGRAM



PIA INTERFACE SIGNALS FOR MPU

The PIA interfaces to the M6800 bus with an 8-bit bidirectional data bus, three chip select lines, two register select lines, two interrupt request lines, a read/write line, an enable line and a reset line. To ensure proper operation with the MC6800, MC6802, or MC6808 microprocessors, VMA should be used as an active part of the address decoding.

Bidirectional Data (D0-D7) — The bidirectional data lines (D0-D7) allow the transfer of data between the MPU and the PIA. The data bus output drivers are three-state devices that remain in the high-impedance (off) state except when the MPU performs a PIA read operation. The read/write line is in the read (high) state when the PIA is selected for a read operation.

Enable (E) — The enable pulse, E, is the only timing signal that is supplied to the PIA. Timing of all other signals is referenced to the leading and trailing edges of the E pulse.

Read/Write (R/$\overline{W}$) — This signal is generated by the MPU to control the direction of data transfers on the data bus. A low state on the PIA read/write line enables the input buffers and data is transferred from the MPU to the PIA on the E signal if the device has been selected. A high on the read/write line sets up the PIA for a transfer of data to the bus. The PIA output buffers are enabled when the proper address and the enable pulse E are present.

$\overline{RESET}$ — The active low $\overline{RESET}$ line is used to reset all register bits in the PIA to a logical zero (low). This line can be used as a power-on reset and as a master reset during system operation.

Chip Selects (CS0, CS1, and $\overline{CS2}$) — These three input signals are used to select the PIA. CS0 and CS1 must be high and $\overline{CS2}$ must be low for selection of the device. Data transfers are then performed under the control of the enable and read/write signals. The chip select lines must be stable for the duration of the E pulse. The device is deselected when any of the chip selects are in the inactive state.

Register Selects (RS0 and RS1) — The two register select lines are used to select the various registers inside the PIA. These two lines are used in conjunction with internal Control Registers to select a particular register that is to be written or read.

The register and chip select lines should be stable for the duration of the E pulse while in the read or write cycle.

Interrupt Request ($\overline{IRQA}$ and $\overline{IRQB}$) — The active low Interrupt Request lines ($\overline{IRQA}$ and $\overline{IRQB}$) act to interrupt the MPU either directly or through interrupt priority circuitry. These lines are "open drain" (no load device on the chip). This permits all interrupt request lines to be tied together in a wire-OR configuration.

Each Interrupt Request line has two internal interrupt flag bits that can cause the Interrupt Request line to go low. Each flag bit is associated with a particular peripheral interrupt line. Also, four interrupt enable bits are provided in the PIA which may be used to inhibit a particular interrupt from a peripheral device.

Servicing an interrupt by the MPU may be accomplished by a software routine that, on a prioritized basis, sequentially reads and tests the two control registers in each PIA for interrupt flag bits that are set.

The interrupt flags are cleared (zeroed) as a result of an MPU Read Peripheral Data Operation of the corresponding data register. After being cleared, the interrupt flag bit cannot be enabled to be set until the PIA is deselected during an E pulse. The E pulse is used to condition the interrupt control lines (CA1, CA2, CB1, CB2). When these lines are used as interrupt inputs, at least one E pulse must occur from the inactive edge to the active edge of the interrupt input signal to condition the edge sense network. If the interrupt flag has been enabled and the edge sense circuit has been properly conditioned, the interrupt flag will be set on the next active transition of the interrupt input pin.

PIA PERIPHERAL INTERFACE LINES

The PIA provides two 8-bit bidirectional data buses and four interrupt/control lines for interfacing to peripheral devices.

Section A Peripheral Data (PA0-PA7) — Each of the peripheral data lines can be programmed to act as an input or output. This is accomplished by setting a "1" in the corresponding Data Direction Register bit for those lines which are to be outputs. A "0" in a bit of the Data Direction Register causes the corresponding peripheral data line to act as an input. During an MPU Read Peripheral Data Operation, the data on peripheral lines programmed to act as inputs appears directly on the corresponding MPU Data Bus lines. In the input mode, the internal pullup resistor on these lines represents a maximum of 1.5 standard TTL loads.

The data in Output Register A will appear on the data lines that are programmed to be outputs. A logical "1" written into the register will cause a "high" on the corresponding data line while a "0" results in a "low." Data in Output Register A may be read by an MPU "Read Peripheral Data A" operation when the corresponding lines are programmed as outputs. This data will be read properly if the voltage on the peripheral data lines is greater than 2.0 volts for a logic "1" output and less than 0.8 volt for a logic "0" output. Loading the output lines such that the voltage on these lines does not reach full voltage causes the data transferred into the MPU on a Read operation to differ from that contained in the respective bit of Output Register A.

Section B Peripheral Data (PB0-PB7) — The peripheral data lines in the B Section of the PIA can be programmed to act as either inputs or outputs in a similar manner to PA0-PA7. They have three-state capabiity, allowing them to enter a high-impedance state when the peripheral data line is used as an input. In addition, data on the peripheral data lines

PB0-PB7 will be read properly from those lines programmed as outputs even if the voltages are below 2.0 volts for a "high" or above 0.8 V for a "low". As outputs, these lines are compatible with standard TTL and may also be used as a source of at least 1 milliampere at 1.5 volts to directly drive the base of a transistor switch.

Interrupt Input (CA1 and CB1) – Peripheral input lines CA1 and CB1 are input only lines that set the interrupt flags of the control registers. The active transition for these signals is also programmed by the two control registers.

Peripheral Control (CA2) – The peripheral control line CA2 can be programmed to act as an interrupt input or as a peripheral control output. As an output, this line is compatible with standard TTL; as an input the internal pullup resistor on this line represents 1.5 standard TTL loads. The function of this signal line is programmed with Control Register A.

Peripheral Control (CB2) – Peripheral Control line CB2 may also be programmed to act as an interrupt input or peripheral control output. As an input, this line has high input impedance and is compatible with standard TTL. As an output it is compatible with standard TTL and may also be used as a source of up to 1 milliampere at 1.5 volts to directly drive the base of a transistor switch. This line is programmed by Control Register B.

3

INTERNAL CONTROLS

INITIALIZATION

A $\overline{\text{RESET}}$ has the effect of zeroing all PIA registers. This will set PA0-PA7, PB0-PB7, CA2 and CB2 as inputs, and all interrupts disabled. The PIA must be configured during the restart program which follows the reset.

There are six locations within the PIA accessible to the MPU data bus: two Peripheral Registers, two Data Direction Registers, and two Control Registers. Selection of these locations is controlled by the RS0 and RS1 inputs together with bit 2 in the Control Register, as shown in Table 1.

Details of possible configurations of the Data Direction and Control Register are as follows:

TABLE 1 – INTERNAL ADDRESSING

RS1	RS0	Control Register Bit CRA-2	Control Register Bit CRB-2	Location Selected
0	0	1	X	Peripheral Register A
0	0	0	X	Data Direction Register A
0	1	X	X	Control Register A
1	0	X	1	Peripheral Register B
1	0	X	0	Data Direction Register B
1	1	X	X	Control Register B

X = Don't Care

PORT A-B HARDWARE CHARACTERISTICS

As shown in Figure 17, the MC6821 has a pair of I/O ports whose characteristics differ greatly. The A side is designed to drive CMOS logic to normal 30% to 70% levels, and incorporates an internal pullup device that remains connected even in the input mode. Because of this, the A side requires more drive current in the input mode than Port B. In contrast, the B side uses a normal three-state NMOS buffer which cannot pullup to CMOS levels without external resistors. The B side can drive extra loads such as Darlingtons without problem. When the PIA comes out of reset, the A port represents inputs with pullup resistors, whereas the B side (input mode also) will float high or low, depending upon the load connected to it.

Notice the differences between a Port A and Port B read operation when in the output mode. When reading Port A, the actual pin is read, whereas the B side read comes from an output latch, ahead of the actual pin.

CONTROL REGISTERS (CRA and CRB)

The two Control Registers (CRA and CRB) allow the MPU to control the operation of the four peripheral control lines CA1, CA2, CB1, and CB2. In addition they allow the MPU to enable the interrupt lines and monitor the status of the interrupt flags. Bits 0 through 5 of the two registers may be written or read by the MPU when the proper chip select and register select signals are applied. Bits 6 and 7 of the two registers are read only and are modified by external interrupts occurring on control lines CA1, CA2, CB1, or CB2. The format of the control words is shown in Figure 18.

DATA DIRECTION ACCESS CONTROL BIT (CRA-2 and CRB-2)

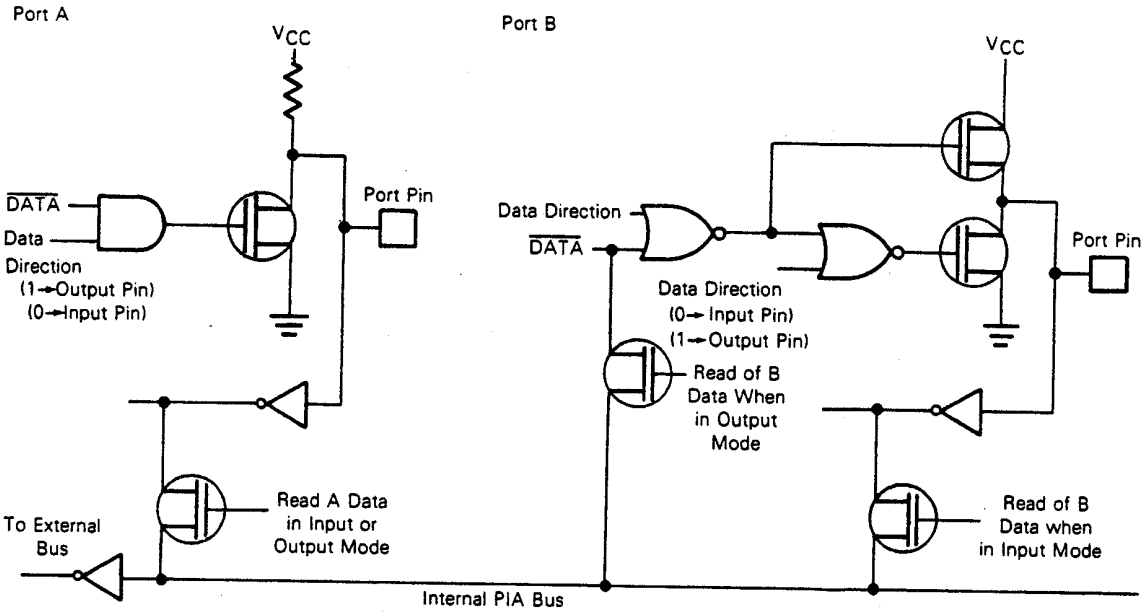
Bit 2, in each Control Register (CRA and CRB), determines selection of either a Peripheral Output Register or the corresponding Data Direction E Register when the proper register select signals are applied to RS0 and RS1. A "1" in bit 2 allows access of the Peripheral Interface Register, while a "0" causes the Data Direction Register to be addressed.

Interrupt Flags (CRA-6, CRA-7, CRB-6, and CRB-7) – The four interrupt flag bits are set by active transitions of signals on the four Interrupt and Peripheral Control lines when those lines are programmed to be inputs. These bits cannot be set directly from the MPU Data Bus and are reset indirectly by a Read Peripheral Data Operation on the appropriate section.

Control of CA2 and CB2 Peripheral Control Lines (CRA-3, CRA-4, CRA-5, CRB-3, CRB-4, and CRB-5) – Bits 3, 4, and 5 of the two control registers are used to control the CA2 and CB2 Peripheral Control lines. These bits determine if the control lines will be an interrupt input or an output control signal. If bit CRA-5 (CRB-5) is low, CA2 (CB2) is an interrupt input line similar to CA1 (CB1). When CRA-5 (CRB-5) is high, CA2 (CB2) becomes an output signal that may be used to control peripheral data transfers. When in the output mode, CA2 and CB2 have slightly different loading characteristics.

Control of CA1 and CB1 Interrupt Input Lines (CRA-0, CRB-0, CRA-1, and CRB-1) — The two lowest-order bits of the control registers are used to control the interrupt input lines CA1 and CB1. Bits CRA-0 and CRB-0 are used to enable the MPU interrupt signals $\overline{IRQA}$ and $\overline{IRQB}$, respectively. Bits CRA-1 and CRB-1 determine the active transition of the interrupt input signals CA1 and CB1.

FIGURE 17 — PORT A AND PORT B EQUIVALENT CIRCUITS



ORDERING INFORMATION

MC68A21CP

- Motorola Integrated Circuit
- M6800 Family
- Blanks = 1.0 MHz
- A = 1.5 MHz
- B = 2.0 MHz
- Device Designation In M6800 Family
- Temperature Range
  - Blank = 0° → +70°C
  - C = −40° → +85°C
- Package
  - P = Plastic
  - S = Cerdip
  - L = Ceramic

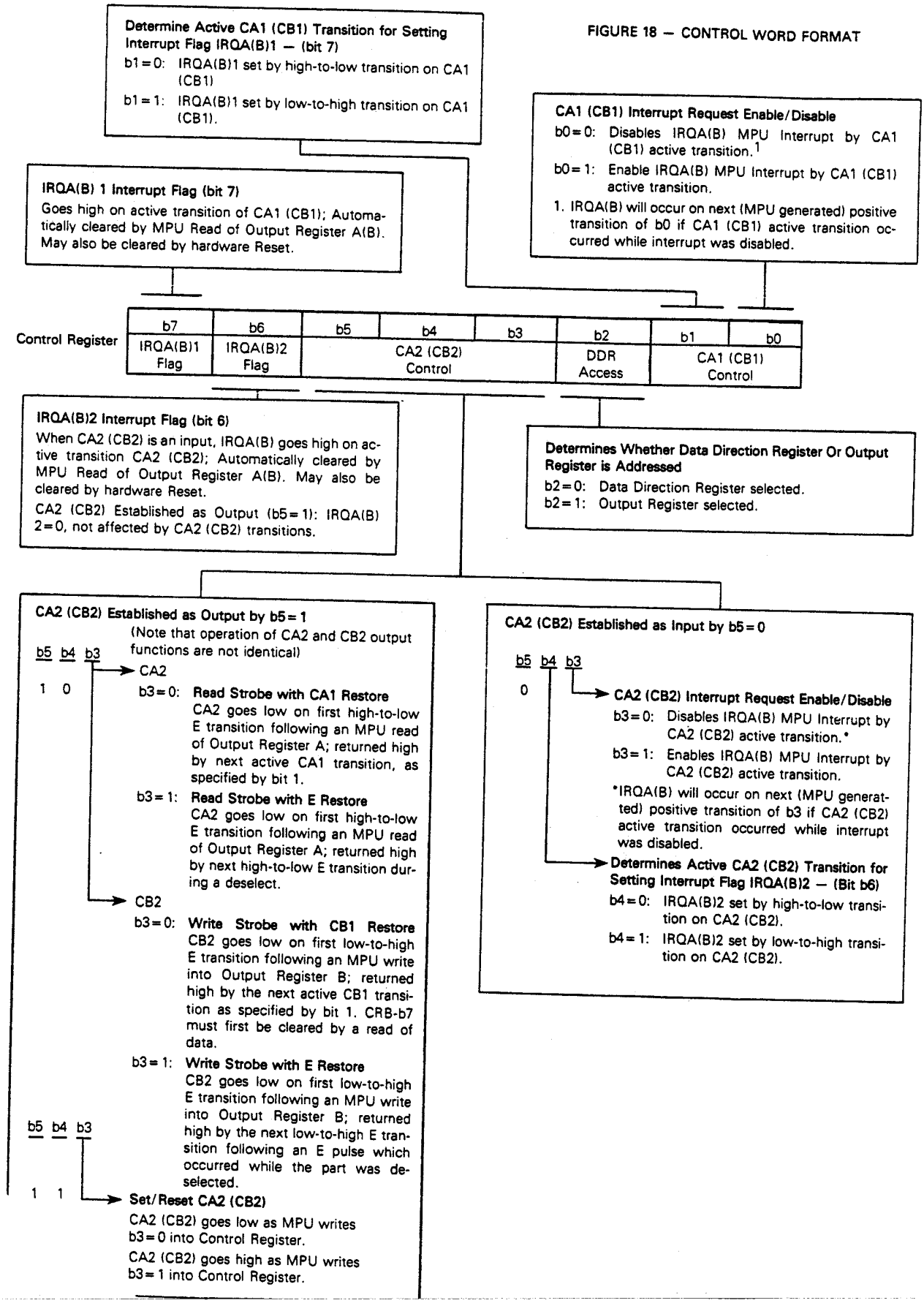
BETTER PROGRAM

Better program processing is available on all types listed. Add suffix letters to part number.

Level 1 add "S" Level 2 add "D" Level 3 add "DS"

Level 1 "S" = 10 Temp Cycles — (−25 to 150°C); Hi Temp testing at T_A max.
Level 2 "D" = 168 Hour Burn-in at 125°C
Level 3 "DS" = Combination of Level 1 and 2.

FIGURE 18 — CONTROL WORD FORMAT



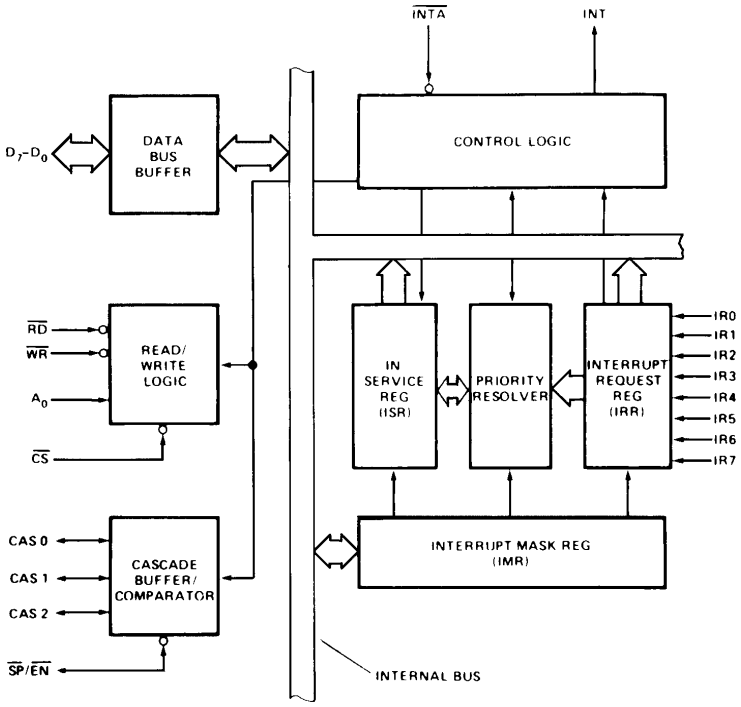
8259A
PROGRAMMABLE INTERRUPT CONTROLLER
(8259A/8259A-2)

- **8086, 8088 Compatible**
- **MCS-80, MCS-85 Compatible**
- **Eight-Level Priority Controller**
- **Expandable to 64 Levels**
- **Programmable Interrupt Modes**
- **Individual Request Mask Capability**
- **Single +5V Supply (No Clocks)**
- **Available in 28-Pin DIP and 28-Lead PLCC Package**
  (See Packaging Spec., Order #231369)
- **Available in EXPRESS**
  — Standard Temperature Range
  — Extended Temperature Range

The Intel 8259A Programmable Interrupt Controller handles up to eight vectored priority interrupts for the CPU. It is cascadable for up to 64 vectored priority interrupts without additional circuitry. It is packaged in a 28-pin DIP, uses NMOS technology and requires a single +5V supply. Circuitry is static, requiring no clock input.

The 8259A is designed to minimize the software and real time overhead in handling multi-level priority interrupts. It has several modes, permitting optimization for a variety of system requirements.

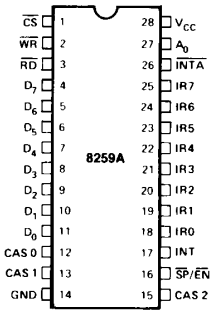
The 8259A is fully upward compatible with the Intel 8259. Software originally written for the 8259 will operate the 8259A in all 8259 equivalent modes (MCS-80/85, Non-Buffered, Edge Triggered).



231468-1

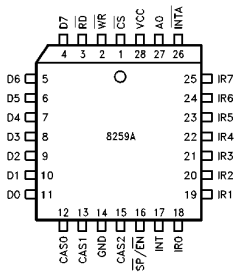
Figure 1. Block Diagram

DIP



231468-2

PLCC



231468-31

Figure 2. Pin Configurations

Table 1. Pin Description

Symbol	Pin No.	Type	Name and Function
V_{CC}	28	I	**SUPPLY:** +5V Supply.
GND	14	I	**GROUND**
$\overline{CS}$	1	I	**CHIP SELECT:** A low on this pin enables $\overline{RD}$ and $\overline{WR}$ communication between the CPU and the 8259A. INTA functions are independent of CS.
$\overline{WR}$	2	I	**WRITE:** A low on this pin when CS is low enables the 8259A to accept command words from the CPU.
$\overline{RD}$	3	I	**READ:** A low on this pin when CS is low enables the 8259A to release status onto the data bus for the CPU.
D_7-D_0	4–11	I/O	**BIDIRECTIONAL DATA BUS:** Control, status and interrupt-vector information is transferred via this bus.
CAS_0-CAS_2	12, 13, 15	I/O	**CASCADE LINES:** The CAS lines form a private 8259A bus to control a multiple 8259A structure. These pins are outputs for a master 8259A and inputs for a slave 8259A.
$\overline{SP}/\overline{EN}$	16	I/O	**SLAVE PROGRAM/ENABLE BUFFER:** This is a dual function pin. When in the Buffered Mode it can be used as an output to control buffer transceivers (EN). When not in the buffered mode it is used as an input to designate a master (SP = 1) or slave (SP = 0).
INT	17	O	**INTERRUPT:** This pin goes high whenever a valid interrupt request is asserted. It is used to interrupt the CPU, thus it is connected to the CPU's interrupt pin.
IR_0-IR_7	18–25	I	**INTERRUPT REQUESTS:** Asynchronous inputs. An interrupt request is executed by raising an IR input (low to high), and holding it high until it is acknowledged (Edge Triggered Mode), or just by a high level on an IR input (Level Triggered Mode).
$\overline{INTA}$	26	I	**INTERRUPT ACKNOWLEDGE:** This pin is used to enable 8259A interrupt-vector data onto the data bus by a sequence of interrupt acknowledge pulses issued by the CPU.
A_0	27	I	**A0 ADDRESS LINE:** This pin acts in conjunction with the $\overline{CS}$, $\overline{WR}$, and $\overline{RD}$ pins. It is used by the 8259A to decipher various Command Words the CPU writes and status the CPU wishes to read. It is typically connected to the CPU A0 address line (A1 for 8086, 8088).

FUNCTIONAL DESCRIPTION

Interrupts in Microcomputer Systems

Microcomputer system design requires that I.O devices such as keyboards, displays, sensors and other components receive servicing in a an efficient manner so that large amounts of the total system tasks can be assumed by the microcomputer with little or no effect on throughput.

The most common method of servicing such devices is the *Polled* approach. This is where the processor must test each device in sequence and in effect ''ask'' each one if it needs servicing. It is easy to see that a large portion of the main program is looping through this continuous polling cycle and that such a method would have a serious detrimental effect on system throughput, thus limiting the tasks that could be assumed by the microcomputer and reducing the cost effectiveness of using such devices.

A more desirable method would be one that would allow the microprocessor to be executing its main program and only stop to service peripheral devices when it is told to do so by the device itself. In effect, the method would provide an external asynchronous input that would inform the processor that it should complete whatever instruction that is currently being executed and fetch a new routine that will service the requesting device. Once this servicing is complete, however, the processor would resume exactly where it left off.

This method is called *Interrupt*. It is easy to see that system throughput would drastically increase, and thus more tasks could be assumed by the microcomputer to further enhance its cost effectiveness.

The Programmable Interrupt Controller (PIC) functions as an overall manager in an Interrupt-Driven system environment. It accepts requests from the peripheral equipment, determines which of the incoming requests is of the highest importance (priority), ascertains whether the incoming request has a higher priority value than the level currently being serviced, and issues an interrupt to the CPU based on this determination.

Each peripheral device or structure usually has a special program or ''routine'' that is associated with its specific functional or operational requirements; this is referred to as a ''service routine''. The PIC, after issuing an Interrupt to the CPU, must somehow input information into the CPU that can ''point'' the Program Counter to the service routine associated with the requesting device. This ''pointer'' is an address in a vectoring table and will often be referred to, in this document, as vectoring data.

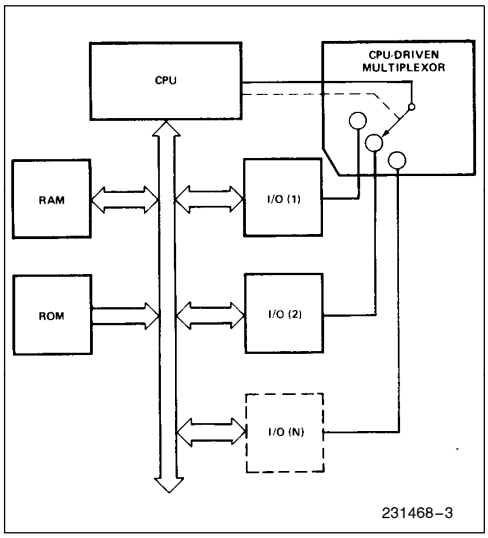


Figure 3a. Polled Method

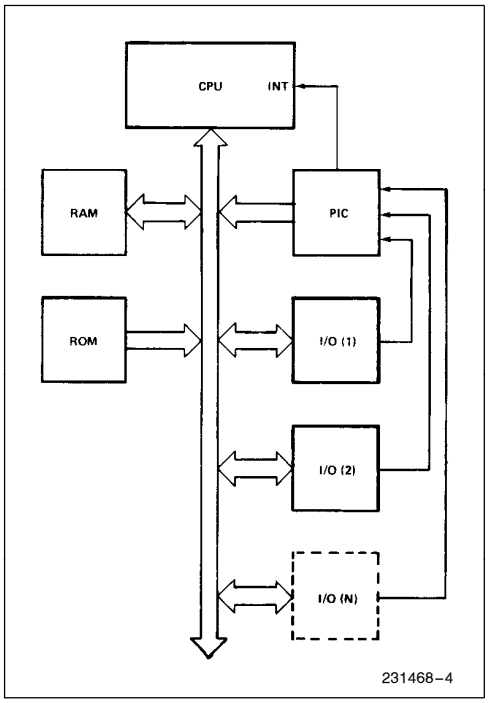


Figure 3b. Interrupt Method

The 8259A is a device specifically designed for use in real time, interrupt driven microcomputer systems. It manages eight levels or requests and has built-in features for expandability to other 8259A's (up to 64 levels). It is programmed by the system's software as an I/O peripheral. A selection of priority modes is available to the programmer so that the manner in which the requests are processed by the 8259A can be configured to match his system requirements. The priority modes can be changed or reconfigured dynamically at any time during the main program. This means that the complete interrupt structure can be defined as required, based on the total system environment.

INTERRUPT REQUEST REGISTER (IRR) AND IN-SERVICE REGISTER (ISR)

The interrupts at the IR input lines are handled by two registers in cascade, the Interrupt Request Register (IRR) and the In-Service (ISR). The IRR is used to store all the interrupt levels which are requesting service; and the ISR is used to store all the interrupt levels which are being serviced.

PRIORITY RESOLVER

This logic block determines the priorites of the bits set in the IRR. The highest priority is selected and strobed into the corresponding bit of the ISR during $\overline{INTA}$ pulse.

INTERRUPT MASK REGISTER (IMR)

The IMR stores the bits which mask the interrupt lines to be masked. The IMR operates on the IRR. Masking of a higher priority input will not affect the interrupt request lines of lower quality.

INT (INTERRUPT)

This output goes directly to the CPU interrupt input. The V_{OH} level on this line is designed to be fully compatible with the 8080A, 8085A and 8086 input levels.

$\overline{INTA}$ (INTERRUPT ACKNOWLEDGE)

$\overline{INTA}$ pulses will cause the 8259A to release vectoring information onto the data bus. The format of this data depends on the system mode (μPM) of the 8259A.

DATA BUS BUFFER

This 3-state, bidirectional 8-bit buffer is used to interface the 8259A to the system Data Bus. Control words and status information are transferred through the Data Bus Buffer.

READ/WRITE CONTROL LOGIC

The function of this block is to accept OUTput commands from the CPU. It contains the Initialization Command Word (ICW) registers and Operation Command Word (OCW) registers which store the various control formats for device operation. This function block also allows the status of the 8259A to be transferred onto the Data Bus.

$\overline{CS}$ (CHIP SELECT)

A LOW on this input enables the 8259A. No reading or writing of the chip will occur unless the device is selected.

$\overline{WR}$ (WRITE)

A LOW on this input enables the CPU to write control words (ICWs and OCWs) to the 8259A.

$\overline{RD}$ (READ)

A LOW on this input enables the 8259A to send the status of the Interrupt Request Register (IRR), In Service Register (ISR), the Interrupt Mask Register (IMR), or the Interrupt level onto the Data Bus.

A_0

This input signal is used in conjunction with $\overline{WR}$ and $\overline{RD}$ signals to write commands into the various command registers, as well as reading the various status registers of the chip. This line can be tied directly to one of the address lines.

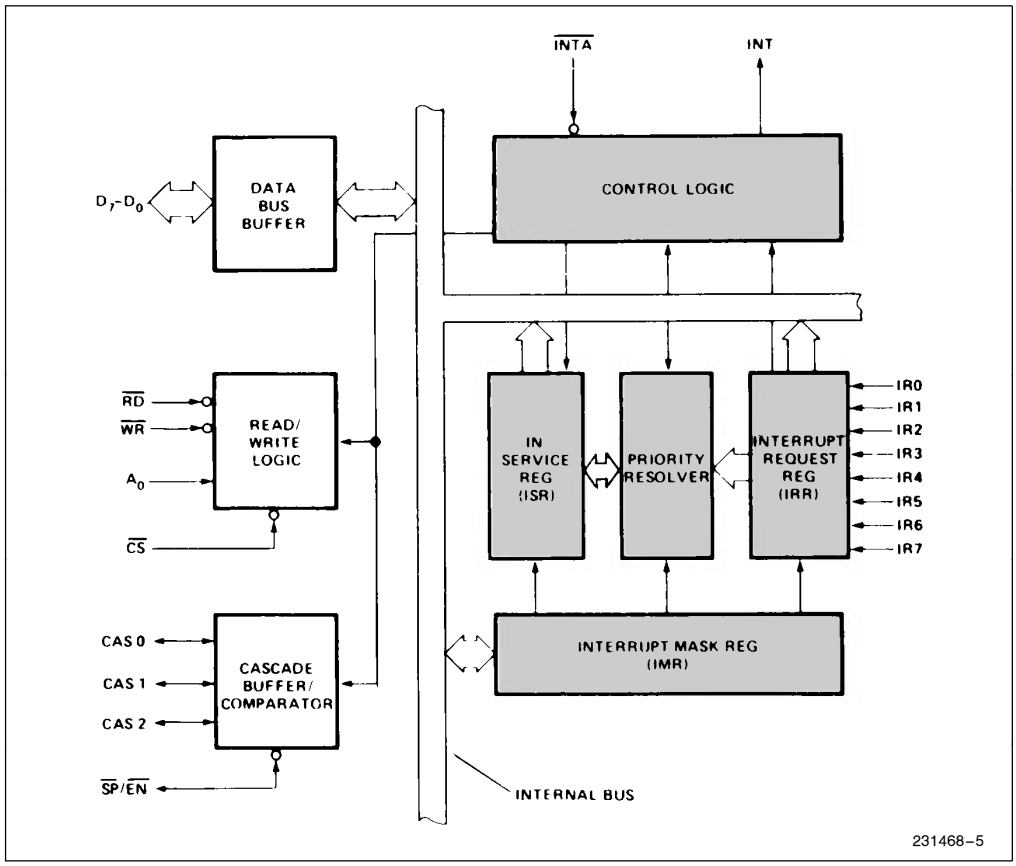


Figure 4a. 8259A Block Diagram

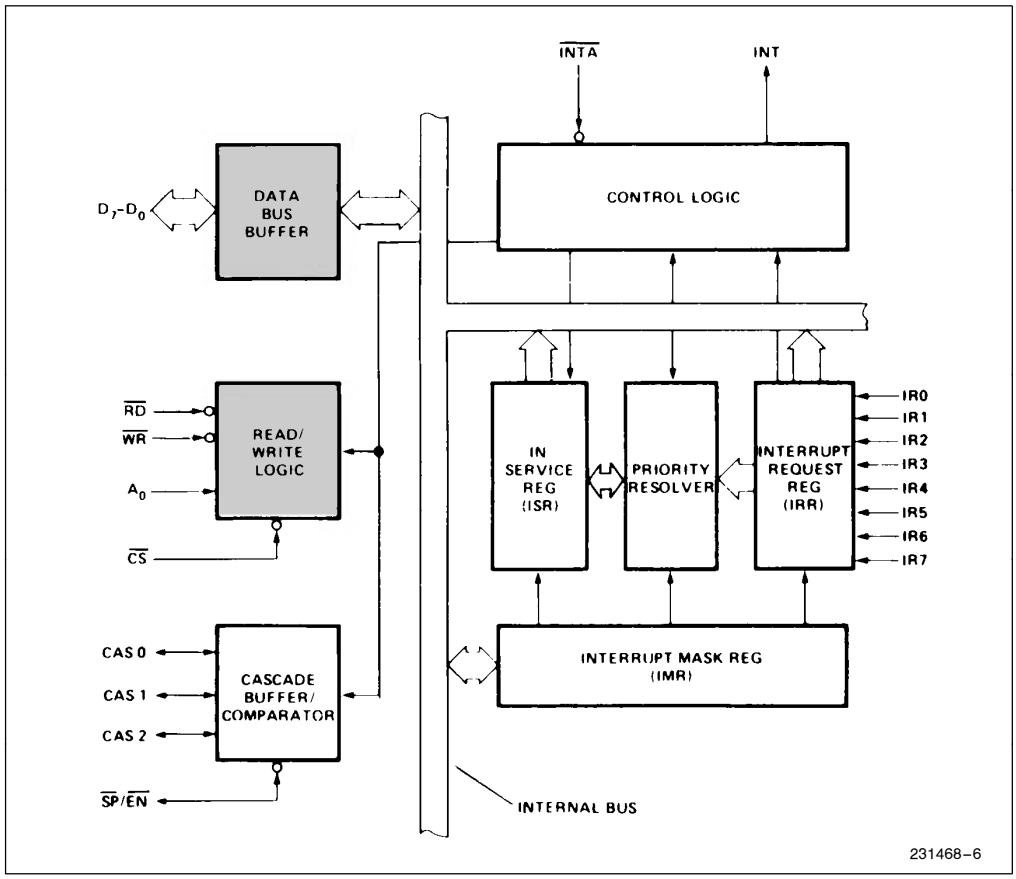


Figure 4b. 8259A Block Diagram

THE CASCADE BUFFER/COMPARATOR

This function block stores and compares the IDs of all 8259A's used in the system. The associated three I/O pins (CAS0-2) are outputs when the 8259A is used as a master and are inputs when the 8259A is used as a slave. As a master, the 8259A sends the ID of the interrupting slave device onto the CAS0–2 lines. The slave thus selected will send its preprogrammed subroutine address onto the Data Bus during the next one or two consecutive $\overline{\text{INTA}}$ pulses. (See section ''Cascading the 8259A''.)

INTERRUPT SEQUENCE

The powerful features of the 8259A in a microcomputer system are its programmability and the interrupt routine addressing capability. The latter allows direct or indirect jumping to the specific interrupt routine requested without any polling of the interrupting devices. The normal sequence of events during an interrupt depends on the type of CPU being used.

The events occur as follows in an MCS-80/85 system:

1. One or more of the INTERRUPT REQUEST lines (IR7–0) are raised high, setting the corresponding IRR bit(s).
2. The 8259A evaluates these requests, and sends an INT to the CPU, if appropriate.
3. The CPU acknowledges the INT and responds with an $\overline{\text{INTA}}$ pulse.
4. Upon receiving an $\overline{\text{INTA}}$ from the CPU group, the highest priority ISR bit is set, and the corresponding IRR bit is reset. The 8259A will also release a CALL instruction code (11001101) onto the 8-bit Data Bus through its D7–0 pins.
5. This CALL instruction will initiate two more $\overline{\text{INTA}}$ pulses to be sent to the 8259A from the CPU group.
6. These two $\overline{\text{INTA}}$ pulses allow the 8259A to release its preprogrammed subroutine address onto the Data Bus. The lower 8-bit address is released at the first $\overline{\text{INTA}}$ pulse and the higher 8-bit address is released at the second $\overline{\text{INTA}}$ pulse.
7. This completes the 3-byte CALL instruction released by the 8259A. In the AEOI mode the ISR bit is reset at the end of the third $\overline{\text{INTA}}$ pulse. Otherwise, the ISR bit remains set until an appropriate EOI command is issued at the end of the interrupt sequence.

The events occuring in an 8086 system are the same until step 4.

4. Upon receiving an $\overline{\text{INTA}}$ from the CPU group, the highest priority ISR bit is set and the corresponding IRR bit is reset. The 8259A does not drive the Data Bus during this cycle.
5. The 8086 will initiate a second $\overline{\text{INTA}}$ pulse. During this pulse, the 8259A releases an 8-bit pointer onto the Data Bus where it is read by the CPU.
6. This completes the interrupt cycle. In the AEOI mode the ISR bit is reset at the end of the second $\overline{\text{INTA}}$ pulse. Otherwise, the ISR bit remains set until an appropriate EOI command is issued at the end of the interrupt subroutine.

If no interrupt request is present at step 4 of either sequence (i.e., the request was too short in duration) the 8259A will issue an interrupt level 7. Both the vectoring bytes and the CAS lines will look like an interrupt level 7 was requested.

When the 8259A PIC receives an interrupt, INT becomes active and an interrupt acknowledge cycle is started. If a higher priority interrupt occurs between the two INTA pulses, the INT line goes inactive immediately after the second INTA pulse. After an unspecified amount of time the INT line is activated again to signify the higher priority interrupt waiting for service. This inactive time is not specified and can vary between parts. The designer should be aware of this consideration when designing a system which uses the 8259A. It is recommended that proper asynchronous design techniques be followed.

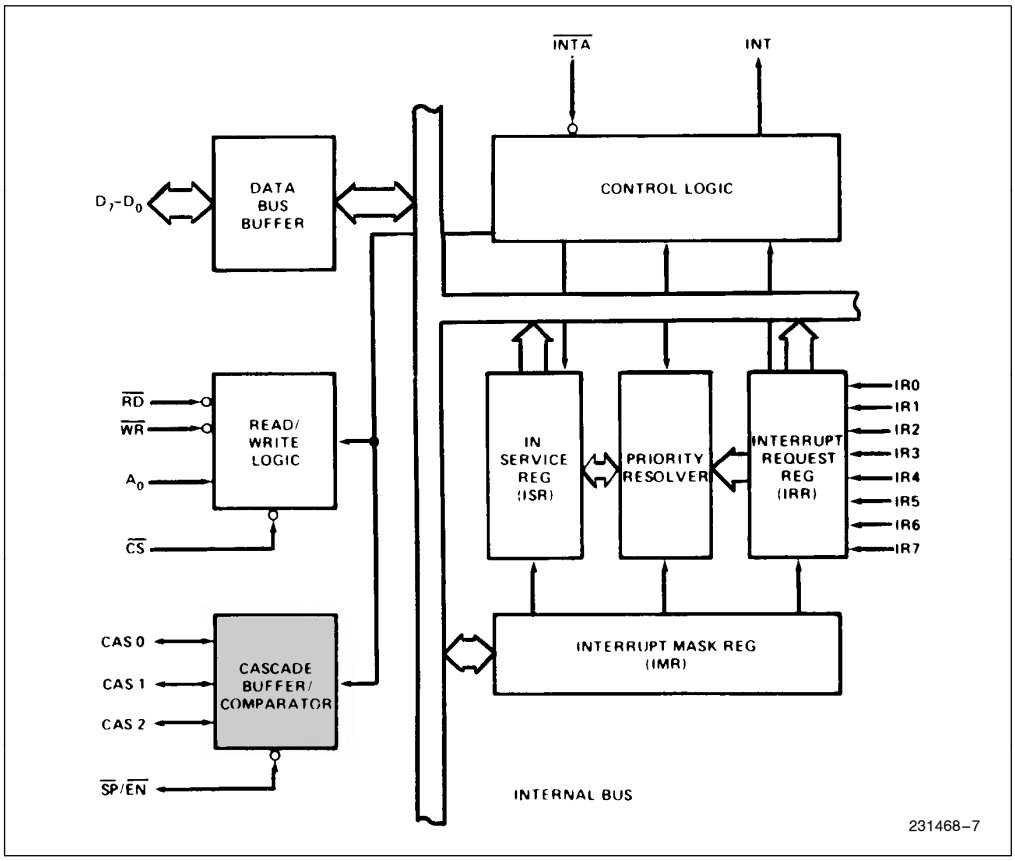


Figure 4c. 8259A Block Diagram

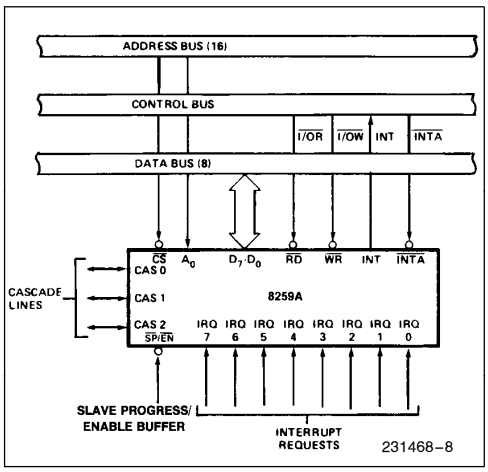


Figure 5. 8259A Interface to Standard System Bus

INTERRUPT SEQUENCE OUTPUTS

MCS-80, MCS-85

This sequence is timed by three $\overline{INTA}$ pulses. During the first $\overline{INTA}$ pulse the CALL opcode is enabled onto the data bus.

Content of First Interrupt Vector Byte

	D7	D6	D5	D4	D3	D2	D1	D0
CALL CODE	1	1	0	0	1	1	0	1

During the second $\overline{INTA}$ pulse the lower address of the appropriate service routine is enabled onto the data bus. When Interval = 4 bits A_5–A_7 are programmed, while A_0–A_4 are automatically inserted by the 8259A. When Interval = 8 only A_6 and A_7 are programmed, while A_0–A_5 are automatically inserted.

Content of Second Interrupt Vector Byte

IR	Interval = 4							
	D7	D6	D5	D4	D3	D2	D1	D0
7	A7	A6	A5	1	1	1	0	0
6	A7	A6	A5	1	1	0	0	0
5	A7	A6	A5	1	0	1	0	0
4	A7	A6	A5	1	0	0	0	0
3	A7	A6	A5	0	1	1	0	0
2	A7	A6	A5	0	1	0	0	0
1	A7	A6	A5	0	0	1	0	0
0	A7	A6	A5	0	0	0	0	0

IR	Interval = 8							
	D7	D6	D5	D4	D3	D2	D1	D0
7	A7	A6	1	1	1	0	0	0
6	A7	A6	1	1	0	0	0	0
5	A7	A6	1	0	1	0	0	0
4	A7	A6	1	0	0	0	0	0
3	A7	A6	0	1	1	0	0	0
2	A7	A6	0	1	0	0	0	0
1	A7	A6	0	0	1	0	0	0
0	A7	A6	0	0	0	0	0	0

During the third $\overline{INTA}$ pulse the higher address of the appropriate service routine, which was programmed as byte 2 of the initialization sequence (A_8–A_{15}), is enabled onto the bus.

Content of Third Interrupt Vector Byte

D7	D6	D5	D4	D3	D2	D1	D0
A15	A14	A13	A12	A11	A10	A9	A8

8086, 8088

8086 mode is similar to MCS-80 mode except that only two Interrupt Acknowledge cycles are issued by the processor and no CALL opcode is sent to the processor. The first interrupt acknowledge cycle is similar to that of MCS-80, 85 systems in that the 8259A uses it to internally freeze the state of the interrupts for priority resolution and as a master it issues the interrupt code on the cascade lines at the end of the $\overline{INTA}$ pulse. On this first cycle it does not issue any data to the processor and leaves its data bus buffers disabled. On the second interrupt acknowledge cycle in 8086 mode the master (or slave if so programmed) will send a byte of data to the processor with the acknowledged interrupt code composed as follows (note the state of the ADI mode control is ignored and A_5–A_{11} are unused in 8086 mode):

Content of Interrupt Vector Byte for 8086 System Mode

	D7	D6	D5	D4	D3	D2	D1	D0
IR7	T7	T6	T5	T4	T3	1	1	1
IR6	T7	T6	T5	T4	T3	1	1	0
IR5	T7	T6	T5	T4	T3	1	0	1
IR4	T7	T6	T5	T4	T3	1	0	0
IR3	T7	T6	T5	T4	T3	0	1	1
IR2	T7	T6	T5	T4	T3	0	1	0
IR1	T7	T6	T5	T4	T3	0	0	1
IR0	T7	T6	T5	T4	T3	0	0	0

PROGRAMMING THE 8259A

The 8259A accepts two types of command words generated by the CPU:

1. *Initialization Command Words (ICWs):* Before normal operation can begin, each 8259A in the system must be brought to a starting point—by a sequence of 2 to 4 bytes timed by $\overline{WR}$ pulses.
2. *Operation Command Words (OCWs):* These are the command words which command the 8259A to operate in various interrupt modes. These modes are:
   a. Fully nested mode
   b. Rotating priority mode
   c. Special mask mode
   d. Polled mode

The OCWs can be written into the 8259A anytime after initialization.

INITIALIZATION COMMAND WORDS (ICWS)

General

Whenever a command is issued with A0 = 0 and D4 = 1, this is interpreted as Initialization Command Word 1 (ICW1). ICW1 starts the intiitalization sequence during which the following automatically occur.

a. The edge sense circuit is reset, which means that following initialization, an interrupt request (IR) input must make a low-to-high transistion to generate an interrupt.

b. The Interrupt Mask Register is cleared.

c. IR7 input is assigned priority 7.

d. The slave mode address is set to 7.

e. Special Mask Mode is cleared and Status Read is set to IRR.

f. If IC4 = 0, then all functions selected in ICW4 are set to zero. (Non-Buffered mode*, no Auto-EOI, MCS-80, 85 system).

***NOTE:**
Master/Slave in ICW4 is only used in the buffered mode.

Initialization Command Words 1 and 2 (ICW1, ICW2)

A_5–A_{15}: *Page starting address of service routines*. In an MCS 80/85 system, the 8 request levels will generate CALLs to 8 locations equally spaced in memory. These can be programmed to be spaced at intervals of 4 or 8 memory locations, thus the 8 routines will occupy a page of 32 or 64 bytes, respectively.

The address format is 2 bytes long (A_0–A_{15}). When the routine interval is 4, A_0–A_4 are automatically inserted by the 8259A, while A_5–A_{15} are programmed externally. When the routine interval is 8, A_0–A_5 are automatically inserted by the 8259A, while A_6–A_{15} are programmed externally.

The 8-byte interval will maintain compatibility with current software, while the 4-byte interval is best for a compact jump table.

In an 8086 system A_{15}–A_{11} are inserted in the five most significant bits of the vectoring byte and the 8259A sets the three least significant bits according to the interrupt level. A_{10}–A_5 are ignored and ADI (Address interval) has no effect.

LTIM: If LTIM = 1, then the 8259A will operate in the level interrupt mode. Edge detect logic on the interrupt inputs will be disabled.

ADI: CALL address interval. ADI = 1 then interval = 4; ADI = 0 then interval = 8.

SNGL: Single. Means that this is the only 8259A in the system. If SNGL = 1 no ICW3 will be issued.

IC4: If this bit is set—ICW4 has to be read. If ICW4 is not needed, set IC4 = 0.

Initialization Command Word 3 (ICW3)

This word is read only when there is more than one 8259A in the system and cascading is used, in which case SNGL = 0. It will load the 8-bit slave register. The functions of this register are:

a. In the master mode (either when SP = 1, or in buffered mode when M/S = 1 in ICW4) a "1" is set for each slave in the system. The master then will release byte 1 of the call sequence (for MCS-80/85 system) and will enable the corresponding slave to release bytes 2 and 3 (for 8086 only byte 2) through the cascade lines.

b. In the slave mode (either when $\overline{SP}$ = 0, or if BUF = 1 and M/S = 0 in ICW4) bits 2–0 identify the slave. The slave compares its cascade input with these bits and, if they are equal, bytes 2 and 3 of the call sequence (or just byte 2 for 8086) are released by it on the Data Bus.

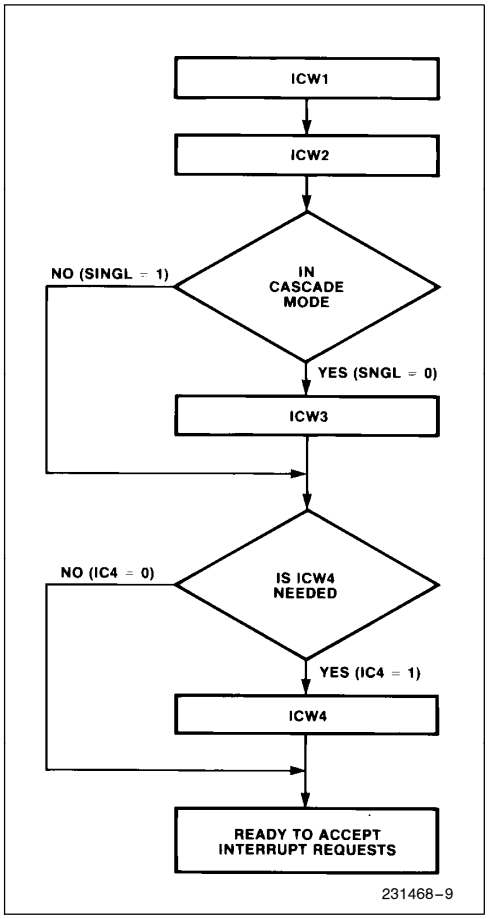


Figure 6. Initialization Sequence

Initialization Command Word 4 (ICW4)

SFNM: If SFNM = 1 the special fully nested mode is programmed.

BUF: If BUF = 1 the buffered mode is programmed. In buffered mode $\overline{SP}/\overline{EN}$ becomes an enable output and the master/slave determination is by M/S.

M/S: If buffered mode is selected: M/S = 1 means the 8259A is programmed to be a master, M/S = 0 means the 8259A is programmed to be a slave. If BUF = 0, M/S has no function.

AEOI: If AEOI = 1 the automatic end of interrupt mode is programmed.

μPM: Microprocessor mode: μPM = 0 sets the 8259A for MCS-80, 85 system operation, μPM = 1 sets the 8259A for 8086 system operation.

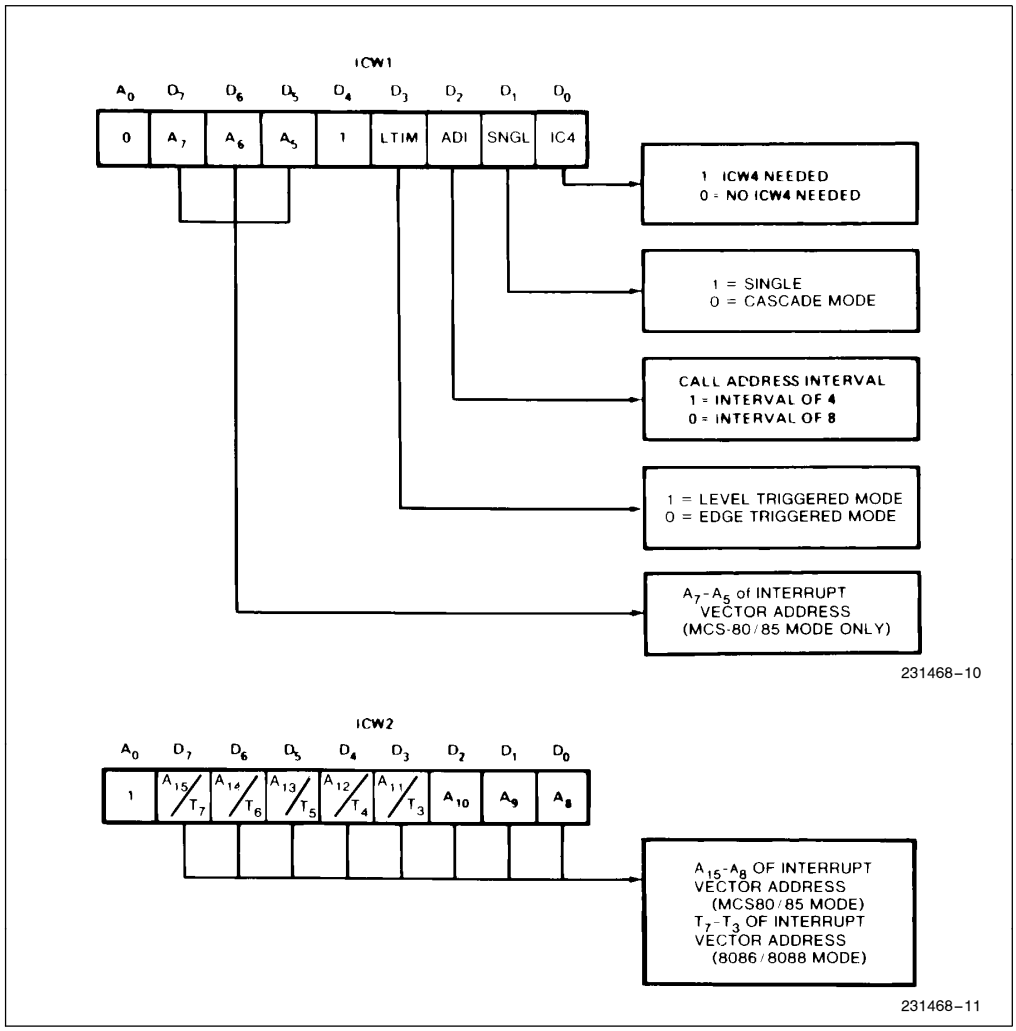
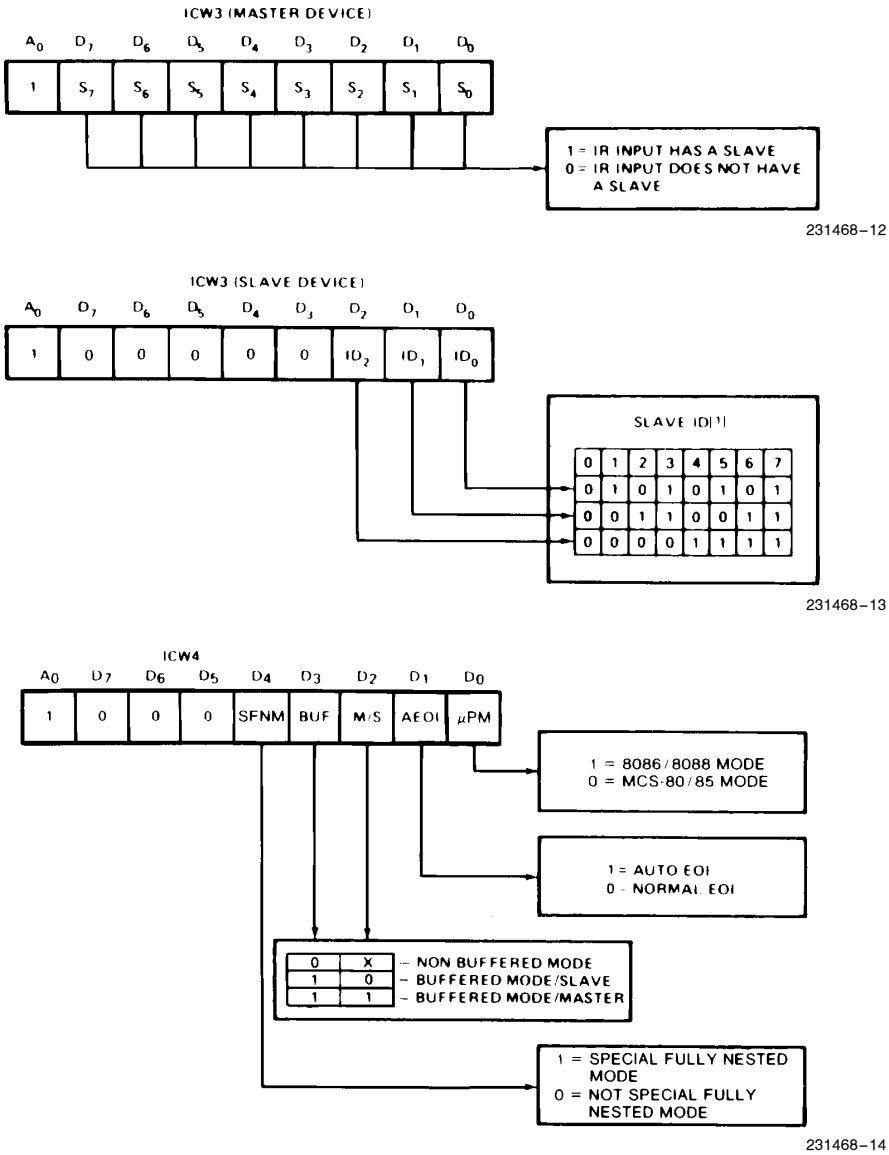


Figure 7. Initialization Command Word Format



NOTE:
Slave ID is equal to the corresponding master IR input.

Figure 7. Initialization Command Word Format (Continued)

OPERATION COMMAND WORDS (OCWS)

After the Initialization Command Words (ICWs) are programmed into the 8259A, the chip is ready to accept interrupt requests at its input lines. However, during the 8259A operation, a selection of algorithms can command the 8259A to operate in various modes through the Operation Command Words (OCWs).

Operation Control Words (OCWs)

OCW1

A0	D7	D6	D5	D4	D3	D2	D1	D0
1	M7	M6	M5	M4	M3	M2	M1	M0

OCW2

0	R	SL	EOI	0	0	L2	L1	L0

OCW3

0	0	ESMM	SMM	0	1	P	RR	RIS

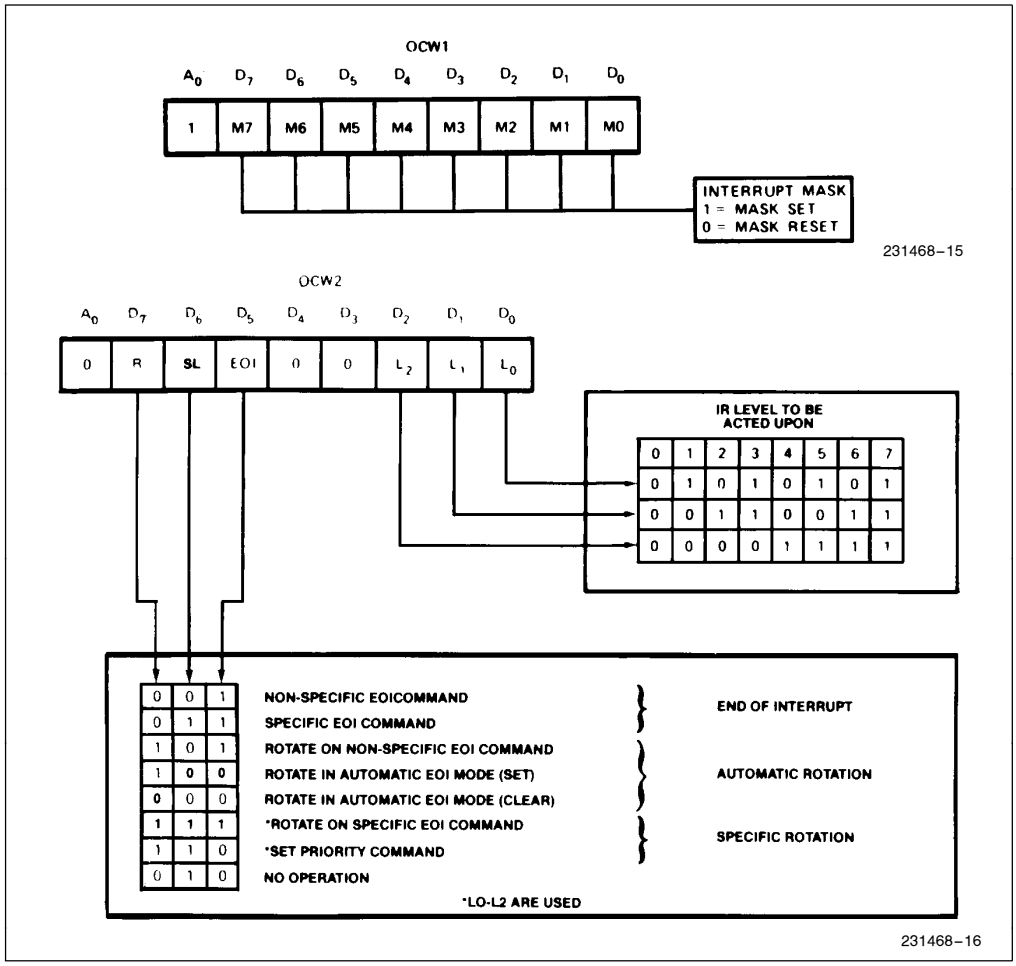


Figure 8. Operation Command Word Format

Operation Control Word 1 (OCW1)

OCW1 sets and clears the mask bits in the interrupt Mask Register (IMR). M_7–M_0 represent the eight mask bits. M = 1 indicates the channel is masked (inhibited), M = 0 indicates the channel is enabled.

Operation Control Word 2 (OCW2)

R, SL, EOI—These three bits control the Rotate and End of Interrupt modes and combinations of the two. A chart of these combinations can be found on the Operation Command Word Format.

L_2, L_1, L_0—These bits determine the interrupt level acted upon when the SL bit is active.

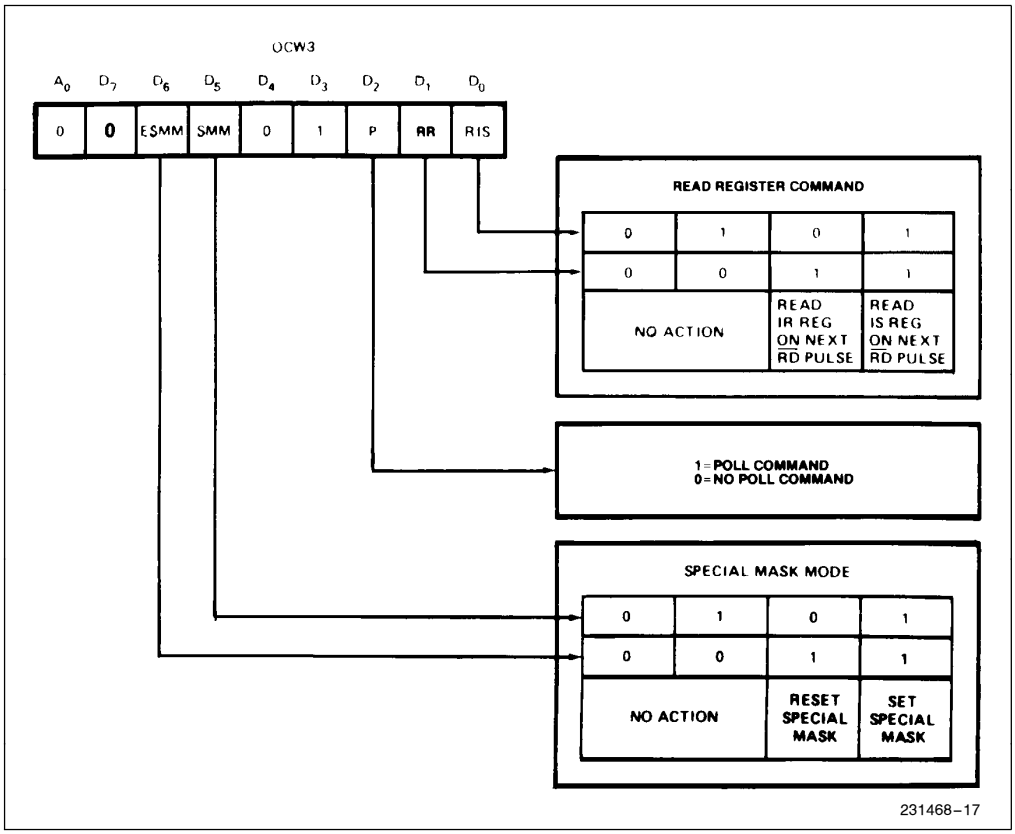


Figure 8. Operation Command Word Format (Continued)

Operation Control Word 3 (OCW3)

ESMM—Enable Special Mask Mode. When this bit is set to 1 it enables the SMM bit to set or reset the Special Mask Mode. When ESMM = 0 the SMM bit becomes a ''don't care''.

SMM—Special Mask Mode. If ESMM = 1 and SMM = 1 the 8259A will enter Special Mask Mode. If ESMM = 1 and SMM = 0 the 8259A will revert to normal mask mode. When ESMM = 0, SMM has no effect.

Fully Nested Mode

This mode is entered after initialization unless another mode is programmed. The interrupt requests are ordered in priority from 0 through 7 (0 highest). When an interrupt is acknowledged the highest priority request is determined and its vector placed on the bus. Additionally, a bit of the Interrupt Service register (ISO-7) is set. This bit remains set until the microprocessor issues an End of Interrupt (EOI) command immediately before returning from the service routine, or if AEOI (Automatic End of Interrupt) bit is set, until the trailing edge of the last INTA. While the IS bit is set, all further interrupts of the same or lower priority are inhibited, while higher levels will generate an interrupt (which will be acknowledged only if the microprocessor internal Interupt enable flip-flop has been re-enabled through software).

After the initialization sequence, IR0 has the highest prioirity and IR7 the lowest. Priorities can be changed, as will be explained, in the rotating priority mode.

End of Interrupt (EOI)

The In Service (IS) bit can be reset either automatically following the trailing edge of the last in sequence $\overline{\text{INTA}}$ pulse (when AEOI bit in ICW1 is set) or by a command word that must be issued to the 8259A before returning from a service routine (EOI command). An EOI command must be issued twice if in the Cascade mode, once for the master and once for the corresponding slave.

There are two forms of EOI command: Specific and Non-Specific. When the 8259A is operated in modes which perserve the fully nested structure, it can determine which IS bit to reset on EOI. When a Non-Specific EOI command is issued the 8259A will automatically reset the highest IS bit of those that are set, since in the fully nested mode the highest IS level was necessarily the last level acknowledged and serviced. A non-specific EOI can be issued with OCW2 (EOI = 1, SL = 0, R = 0).

When a mode is used which may disturb the fully nested structure, the 8259A may no longer be able to determine the last level acknowledged. In this case a Specific End of Interrupt must be issued which includes as part of the command the IS level to be reset. A specific EOI can be issued with OCW2 (EOI = 1, SL = 1, R = 0, and L0–L2 is the binary level of the IS bit to be reset).

It should be noted that an IS bit that is masked by an IMR bit will not be cleared by a non-specific EOI if the 8259A is in the Special Mask Mode.

Automatic End of Interrupt (AEOI) Mode

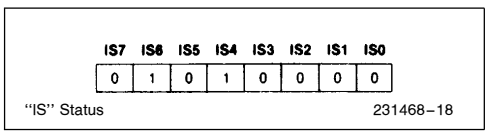
If AEOI = 1 in ICW4, then the 8259A will operate in AEOI mode continuously until reprogrammed by ICW4. in this mode the 8259A will automatically perform a non-specific EOI operation at the trailing edge of the last interrupt acknowledge pulse (third pulse in MCS-80/85, second in 8086). Note that from a system standpoint, this mode should be used only when a nested multilevel interrupt structure is not required within a single 8259A.

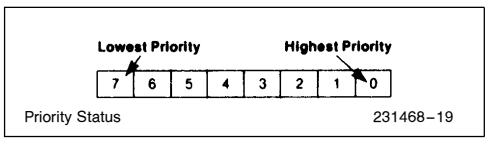
The AEOI mode can only be used in a master 8259A and not a slave. 8259As with a copyright date of 1985 or later will operate in the AEOI mode as a master or a slave.

Automatic Rotation (Equal Priority Devices)

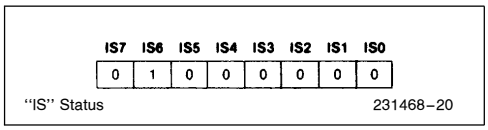
In some applications there are a number of interrupting devices of equal priority. In this mode a device, after being serviced, receives the lowest priority, so a device requesting an interrupt will have to wait, in the worst case until each of 7 other devices are serviced at most *once*. For example, if the priority and ''in service'' status is:

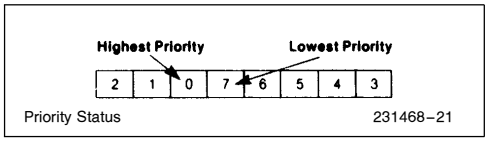
Before Rotate (IR4 the highest prioirity requiring service)





After Rotate (IR4 was serviced, all other priorities rotated correspondingly)





There are two ways to accomplish Automatic Rotation using OCW2, the Rotation on Non-Specific EOI Command (R = 1, SL = 0, EOI = 1) and the Rotate in Automatic EOI Mode which is set by (R = 1, SL = 0, EOI = 0) and cleared by (R = 0, SL = 0, EOI = 0).

Specific Rotation (Specific Priority)

The programmer can change priorities by programming the bottom priority and thus fixing all other priorities; i.e., if IR5 is programmed as the bottom priority device, then IR6 will have the highest one.

The Set Priority command is issued in OCW2 where: R = 1, SL = 1, L0–L2 is the binary priority level code of the bottom priority device.

Observe that in this mode internal status is updated by software control during OCW2. However, it is independent of the End of Interrupt (EOI) command (also executed by OCW2). Priority changes can be executed during an EOI command by using the Rotate on Specific EOI command in OCW2 (R = 1, SL = 1, EOI = 1 and LO–L2 = IR level to receive bottom priority).

Interrupt Masks

Each Interrupt Request input can bem masked individually by the Interrupt Mask Register (IMR) programmed through OCW1. Each bit in the IMR masks one interrupt channel if it is set (1). Bit 0 masks IR0, Bit 1 masks IR1 and so forth. Masking an IR channel does not affect the other channels operation.

Special Mask Mode

Some applications may require an interrupt service routine to dynamically alter the system priority structure during its execution under software control. For example, the routine may wish to inhibit lower priority requests for a portion of its execution but enable some of them for another portion.

The difficulty here is that if an Interrupt Request is acknowledged and an End of Interrupt command did not reset its IS bit (i.e., while executing a service routine), the 8259A would have inhibited all lower priority requests with no easy way for the routine to enable them.

That is where the Special Mask Mode comes in. In the special Mask Mode, when a mask bit is set in OCW1, it inhibits further interrupts at that level *and enables* interrupts from *all other* levels (lower as well as higher) that are not masked.

Thus, any interrupts may be selectively enabled by loading the mask register.

The special Mask Mode is set by OWC3 where: SSMM = 1, SMM = 1, and cleared where SSMM = 1, SMM = 0.

Poll Command

In Poll mode the INT output functions as it normally does. The microprocessor should ignore this output. This can be accomplished either by not connecting the INT output or by masking interrupts within the microprocessor, thereby disabling its interrupt input. Service to devices is achieved by software using a Poll command.

The Poll command is issued by setting P = '1'' in OCW3. The 8259A treats the next $\overline{RD}$ pulse to the 8259A (i.e., $\overline{RD}$ = 0, $\overline{CS}$ = 0) as an interrupt acknowledge, sets the appropriate IS bit if there is a request, and reads the priority level. Interrupt is frozen from $\overline{WR}$ to $\overline{RD}$.

The word enabled onto the data bus during $\overline{RD}$ is:

D7	D6	D5	D4	D3	D2	D1	D0
I	—	—	—	—	W2	W1	W0

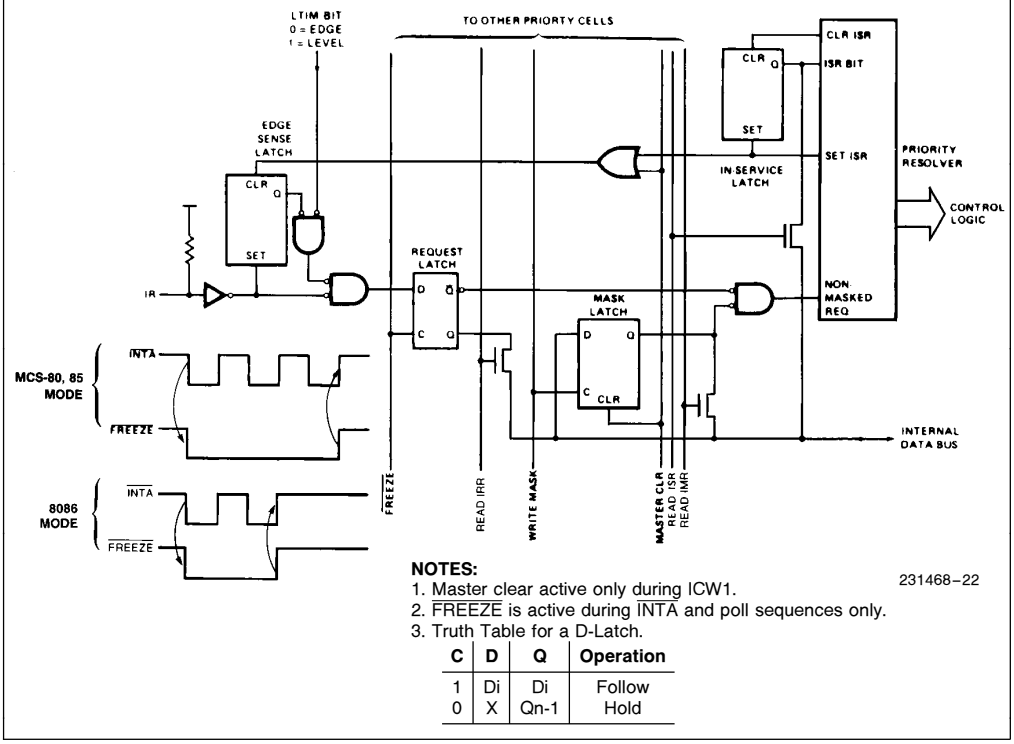
W0–W2: Binary code of the highest priority level requesting service.

I: Equal to ''1'' if there is an interrupt.

This mode is useful if there is a routine command common to several levels so that the $\overline{INTA}$ sequence is not needed (saves ROM space). Another application is to use the poll mode to expand the number of priority levels to more than 64.

Reading the 8259A Status

The input status of several internal registers can be read to update the user information on the system.



NOTES:
1. Master clear active only during ICW1.
2. $\overline{\text{FREEZE}}$ is active during $\overline{\text{INTA}}$ and poll sequences only.
3. Truth Table for a D-Latch.

C	D	Q	Operation
1	Di	Di	Follow
0	X	Qn-1	Hold

Figure 9. Priority Cell—Simplified Logic Diagram

The following registers can be read via OCW3 (IRR and ISR or OCW1 [IMR]).

Interrupt Request Register (IRR): 8-bit register which contains the levels requesting an interrupt to be acknowledged. The highest request level is reset from the IRR when an interrupt is acknowledged. (Not affected by IMR.)

In-Service Register (ISR): 8-bit register which contains the priority levels that are being serviced. The ISR is updated when an End of Interrupt Command is issued.

Interrupt Mask Register: 8-bit register which contains the interrupt request lines which are masked.

The IRR can be read when, prior to the RD pulse, a Read Register Command is issued with OCW3 (RR = 1, RIS = 0.)

The ISR can be read, when, prior to the RD pulse, a Read Register Command is issued with OCW3 (RR = 1, RIS = 1).

There is no need to write an OCW3 before every status read operation, as long as the status read corresponds with the previous one; i.e., the 8259A ''remembers'' whether the IRR or ISR has been previously selected by the OCW3. This is not true when poll is used.

After initialization the 8259A is set to IRR.

For reading the IMR, no OCW3 is needed. The output data bus will contain the IMR whenever $\overline{\text{RD}}$ is active and A0 = 1 (OCW1).

Polling overrides status read when P = 1, RR = 1 in OCW3.

Edge and Level Triggered Modes

This mode is programmed using bit 3 in ICW1.

If LTIM = '0', an interrupt request will be recognized by a low to high transition on an IR input. The IR input can remain high without generating another interrupt.

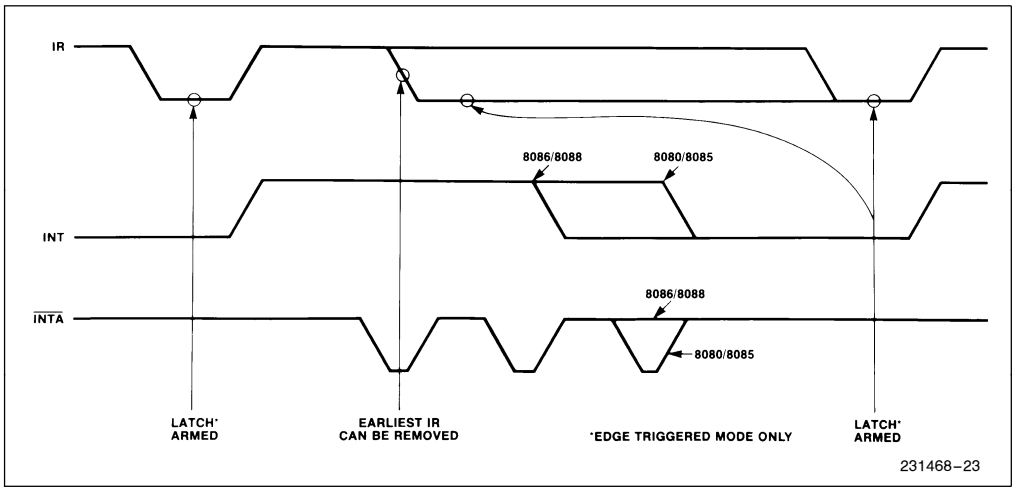


Figure 10. IR Triggering Timing Requirements

If LTIM = '1', an interrupt request will be recognized by a 'high' level on IR Input, and there is no need for an edge detection. The interrupt request must be removed before the EOI command is issued or the CPU interrupts is enabled to prevent a second interrupt from occurring.

The priority cell diagram shows a conceptual circuit of the level sensitive and edge sensitive input circuitry of the 8259A. Be sure to note that the request latch is a transparent D type latch.

In both the edge and level triggered modes the IR inputs must remain high until after the falling edge of the first $\overline{INTA}$. If the IR input goes low before this time a DEFAULT IR7 will occur when the CPU acknowledges the interrupt. This can be a useful safeguard for detecting interrupts caused by spurious noise glitches on the IR inputs. To implement this feature the IR7 routine is used for ''clean up'' simply executing a return instruction, thus ignoring the interrupt. If IR7 is needed for other purposes a default IR7 can still be detected by reading the ISR. A normal IR7 interrupt will set the corresponding ISR bit, a default IR7 won't. If a default IR7 routine occurs during a normal IR7 routine, however, the ISR will remain set. In this case it is necessary to keep track of whether or not the IR7 routine was previously entered. If another IR7 occurs it is a default.

The Special Fully Nest Mode

This mode will be used in the case of a big system where cascading is used, and the priority has to be conserved within each slave. In this case the fully nested mode will be programmed to the master (using ICW4). This mode is similar to the normal nested mode with the following exceptions:

a. When an interrupt request from a certain slave is in service this slave is not locked out from the master's priority logic and further interrupt requests from higher priority IR's within the slave will be recognized by the master and will initiate interrupts to the processor. (In the normal nested mode a slave is masked out when its request is in service and no higher requests from the same slave can be serviced.)

b. When exiting the Interrupt Service routine the software has to check whether the interrupt serviced was the only one from that slave. This is done by sending a non-specific End of Interrupt (EOI) command to the slave and then reading its In-Service register and checking for zero. If it is empty, a non-specific EOI can be sent to the master too. If not, no EOI should be sent.

Buffered Mode

When the 8259A is used in a large system where bus driving buffers are required on the data bus and the cascading mode is used, there exists the problem of enabling buffers.

The buffered mode will structure the 8259A to send an enable signal on $\overline{SP}/\overline{EN}$ to enable the buffers. In this mode, whenever the 8259A's data bus outputs are enabled, the $\overline{SP}/\overline{EN}$ output becomes active.

This modification forces the use of software programming to determine whether the 8259A is a master or a slave. Bit 3 in ICW4 programs the buffered mode, and bit 2 in ICW4 determines whether it is a master or a slave.

CASCADE MODE

The 8259A can be easily interconnected in a system of one master with up to eight slaves to handle up to 64 priority levels.

The master controls the slaves through the 3 line cascade bus. The cascade bus acts like chip selects to the slaves during the $\overline{INTA}$ sequence.

In a cascade configuration, the slave interrupt outputs are connected to the master interrupt request inputs. When a slave request line is activated and afterwards acknowledged, the master will enable the corresponding slave to release the device routine address during bytes 2 and 3 of $\overline{INTA}$. (Byte 2 only for 8086/8088).

The cascade bus lines are normally low and will contain the slave address code from the trailing edge of the first $\overline{INTA}$ pulse to the trailing edge of the third pulse. Each 8259A in the system must follow a separate initialization sequence and can be programmed to work in a different mode. An EOI command must be issued twice: once for the master and once for the corresponding slave. An address decoder is required to activate the Chip Select (CS) input of each 8259A.

The cascade lines of the Master 8259A are activated only for slave inputs, non-slave inputs leave the cascade line inactive (low).

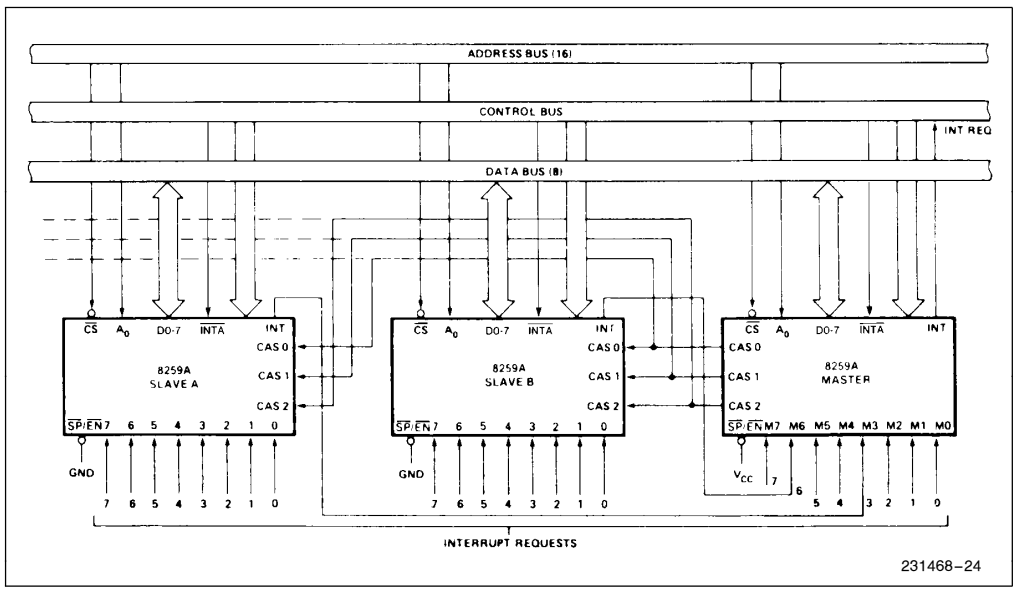


Figure 11. Cascading the 8259A

ABSOLUTE MAXIMUM RATINGS*

Ambient Temperature Under Bias . . . . . 0°C to 70°C
Storage Temperature . . . . . −65°C to +150°C
Voltage on Any Pin
with Respect to Ground . . . . . −0.5V to +7V
Power Dissipation 1W

NOTICE: This is a production data sheet. The specifications are subject to change without notice.

**WARNING: Stressing the device beyond the "Absolute Maximum Ratings" may cause permanent damage. These are stress ratings only. Operation beyond the "Operating Conditions" is not recommended and extended exposure beyond the "Operating Conditions" may affect device reliability.*

D.C. CHARACTERISTICS T_A = 0°C to 70°C, V_{CC} = 5V ± 10%

Symbol	Parameter	Min	Max	Units	Test Conditions
V_{IL}	Input Low Voltage	−0.5	0.8	V	
V_{IH}	Input High Voltage	2.0*	V_{CC} + 0.5V	V	
V_{OL}	Output Low Voltage		0.45	V	I_{OL} = 2.2 mA
V_{OH}	Output High Voltage	2.4		V	I_{OH} = −400 μA
$V_{OH(INT)}$	Interrupt Output High Voltage	3.5		V	I_{OH} = −100 μA
		2.4		V	I_{OH} = −400 μA
I_{LI}	Input Load Current	−10	+10	μA	0V ≤ V_{IN} ≤ V_{CC}
I_{LOL}	Output Leakage Current	−10	+10	μA	0.45V ≤ V_{OUT} ≤ V_{CC}
I_{CC}	V_{CC} Supply Current		85	mA	
I_{LIR}	IR Input Load Current		−300	μA	V_{IN} = 0
			10	μA	V_{IN} = V_{CC}

***NOTE:**
For Extended Temperature EXPRESS V_{IH} = 2.3V.

CAPACITANCE T_A = 25°C; V_{CC} = GND = 0V

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
C_{IN}	Input Capacitance			10	pF	fc = 1 MHz
$C_{I/O}$	I/O Capacitance			20	pF	Unmeasured Pins Returned to V_{SS}

A.C. CHARACTERISTICS $T_A = 0°C$ to $70°C$, $V_{CC} = 5V \pm 10\%$

TIMING REQUIREMENTS

Symbol	Parameter	8259A		8259A-2		Units	Test Conditions
		Min	Max	Min	Max		
TAHRL	AO/$\overline{CS}$ Setup to $\overline{RD}$/$\overline{INTA}$ ↓	0		0		ns	
TRHAX	AO/$\overline{CS}$ Hold after $\overline{RD}$/$\overline{INTA}$ ↑	0		0		ns	
TRLRH	$\overline{RD}$ Pulse Width	235		160		ns	
TAHWL	AO/$\overline{CS}$ Setup to $\overline{WR}$ ↓	0		0		ns	
TWHAX	AO/$\overline{CS}$ Hold after $\overline{WR}$ ↑	0		0		ns	
TWLWH	$\overline{WR}$ Pulse Width	290		190		ns	
TDVWH	Data Setup to $\overline{WR}$ ↑	240		160		ns	
TWHDX	Data Hold after $\overline{WR}$ ↑	0		0		ns	
TJLJH	Interrupt Request Width (Low)	100		100		ns	See Note 1
TCVIAL	Cascade Setup to Second or Third $\overline{INTA}$ ↓ (Slave Only)	55		40		ns	
TRHRL	End of $\overline{RD}$ to Next $\overline{RD}$ End of $\overline{INTA}$ to Next $\overline{INTA}$ within an $\overline{INTA}$ Sequence Only	160		100		ns	
TWHWL	End of $\overline{WR}$ to Next $\overline{WR}$	190		100		ns	
*TCHCL	End of Command to Next Command (Not Same Command Type)	500		150		ns	
	End of $\overline{INTA}$ Sequence to Next $\overline{INTA}$ Sequence.	500		300			

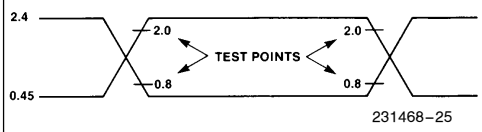
*Worst case timing for TCHCL in an actual microprocessor system is typically much greater than 500 ns (i.e. 8085A = 1.6 μs, 8085A-2 = 1 μs, 8086 = 1 μs, 8086-2 = 625 ns)

NOTE:
This is the low time required to clear the input latch in the edge triggered mode.

TIMING RESPONSES

Symbol	Parameter	8259A		8259A-2		Units	Test Conditions
		Min	Max	Min	Max		
TRLDV	Data Valid from $\overline{RD}$/$\overline{INTA}$ ↓		200		120	ns	C of Data Bus = 100 pF
TRHDZ	Data Float after $\overline{RD}$/$\overline{INTA}$ ↑	10	100	10	85	ns	C of Data Bus Max Test C = 100 pF Min Test C = 15 pF
TJHIH	Interrupt Output Delay		350		300	ns	
TIALCV	Cascade Valid from First $\overline{INTA}$ ↓ (Master Only)		565		360	ns	C_{INT} = 100 pF
TRLEL	Enable Active from $\overline{RD}$ ↓ or $\overline{INTA}$ ↓		125		100	ns	$C_{CASCADE}$ = 100 pF
TRHEH	Enable Inactive from $\overline{RD}$ ↑ or $\overline{INTA}$ ↑		150		150	ns	
TAHDV	Data Valid from Stable Address		200		200	ns	
TCVDV	Cascade Valid to Valid Data		300		200	ns	

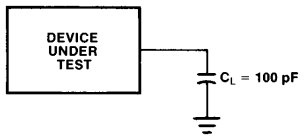
A.C. TESTING INPUT/OUTPUT WAVEFORM



231468–25

A.C. Testing: Inputs are driven at 2.4V for a logic "1" and 0.45V for a logic "0". Timing measurements are made at 2.0V for a logic "1" and 0.8V for a logic "0".

A.C. TESTING LOAD CIRCUIT

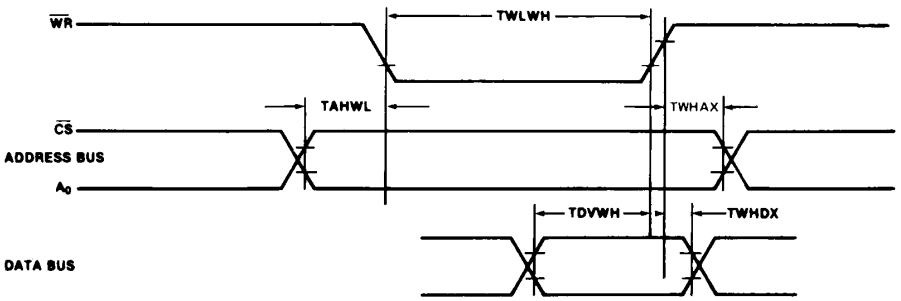


231468–26

C_L = 100 pF
C_L Includes Jig Capacitance

WAVEFORMS

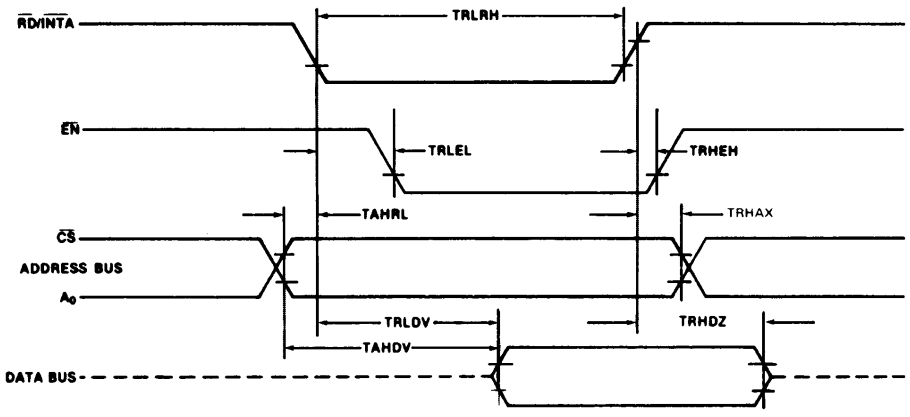
WRITE



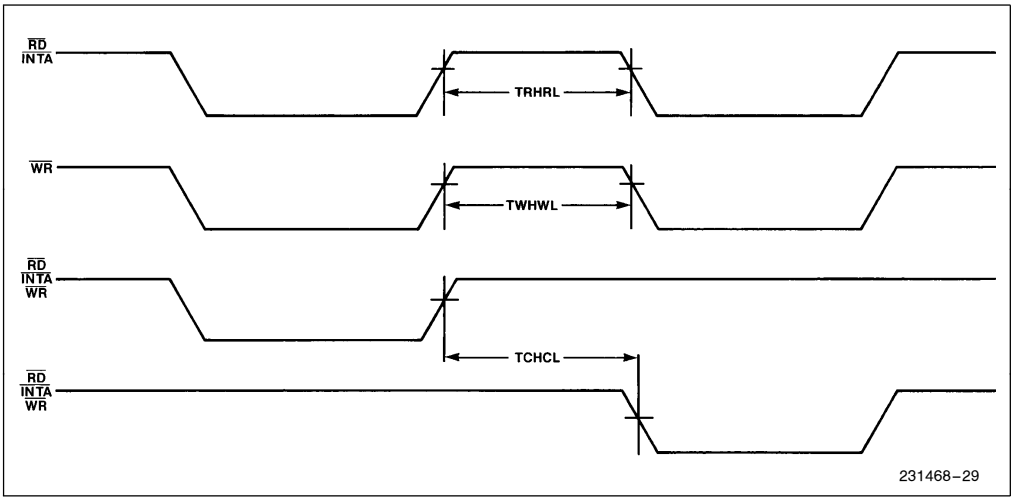
231468–27

WAVEFORMS (Continued)

READ/INTA

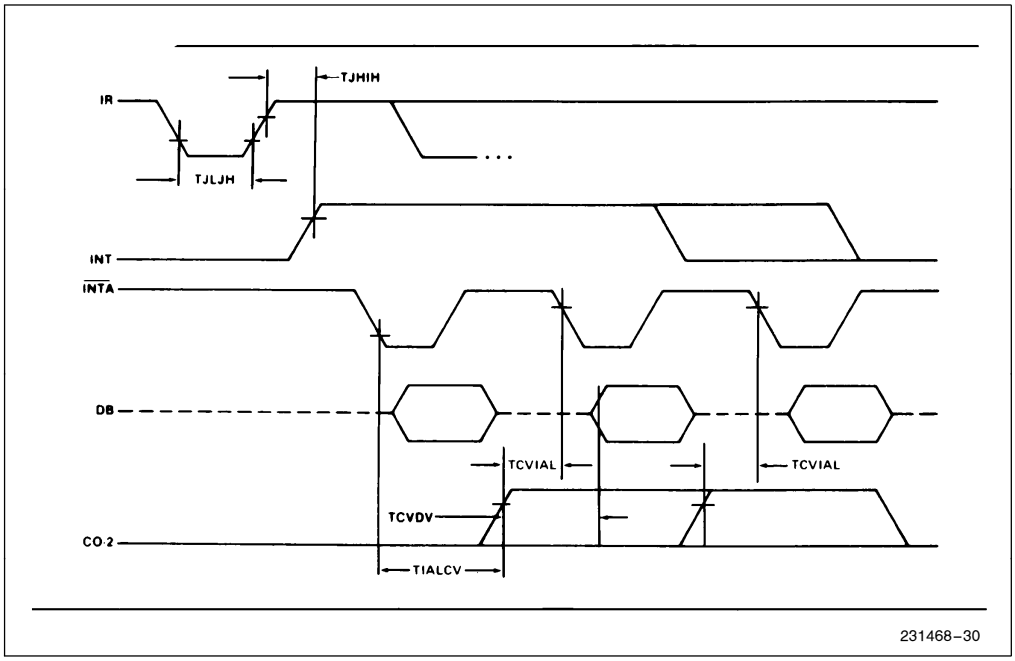


OTHER TIMING



WAVEFORMS (Continued)

$\overline{\text{INTA}}$ SEQUENCE



NOTES:
Interrupt output must remain HIGH at least until leading edge of first $\overline{\text{INTA}}$.
1. Cycle 1 in 8086, 8088 systems, the Data Bus is not active.

Data Sheet Revision Review

The following changes have been made since revision 2 of the 8259A data sheet.

1. The first paragraph of the Poll Command section was rewritten to clarify the status of the INT pin.
2. A paragraph was added to the Interrupt Sequence section to indicate the status of the INT pin during multiple interrupts.
3. A reference to PLCC packaging was added.
4. All references to the 8259A-8 have been deleted.

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Printed in U.S.A./xxxx/1196/B10M/xx xx

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PRODUCT USER MANUAL

GPS RECEIVER ENGINE BOARD

EM-406A

GlobalSat Technology Corporation

¥x¥_¿¤¤¤©M¥««Ø¤@186 ¸¹ 16 ¼Ó(»·ªF¥@¬ö¼s³õ

16, No.186,Chien 1 Road, 235Chung Ho City,Taipei Hsien, Taiwan ,R.O.C.

Tel: 886-2-8226-3799(Rep.) **Fax: 886-2-8226-3899**

Web: www.globalsat.com.tw **E-mail:service@globalsat.com.tw**

Features:

SiRF star¢» high performance GPS Chip Set
Very high sensitivity (Tracking Sensitivity: -159 dBm)
Extremely fast TTFF (Time To First Fix) at low signal level
Support NMEA 0183 data protocol
Built-in SuperCap to reserve system data for rapid satellite acquisition
Built-in patch antenna
LED indicator for GPS fix or not fix

LED OFF:	Receiver switch off
LED ON:	No fixed, Signal searching
LED Flashing:	Position Fixed

Specification:

General

Chipset	SiRF Star¢»
Frequency	L1, 1575.42 MHz
C/A code	1.023 MHz chip rate
Channels	20 channel all-in-view tracking
Sensitivity	-159 dBm

Accuracy

Position	10 meters, 2D RMS
	5 meters, 2D RMS, WAAS enabled
Velocity	0.1 m/s
Time	1us synchronized to GPS time

Datum

Default	WGS-84

Acquisition Time

Reacquisition	0.1 sec., average
Hot start	1 sec., average
Warm start	38 sec., average
Cold start	42 sec., average

Dynamic Conditions

Altitude	18,000 meters (60,000 feet) max
Velocity	515 meters /second (1000 knots) max
Acceleration	Less than 4g
Jerk	20m/sec **3

Power

Main power input	4.5V ~ 6.5V DC input
Power consumption	44mA

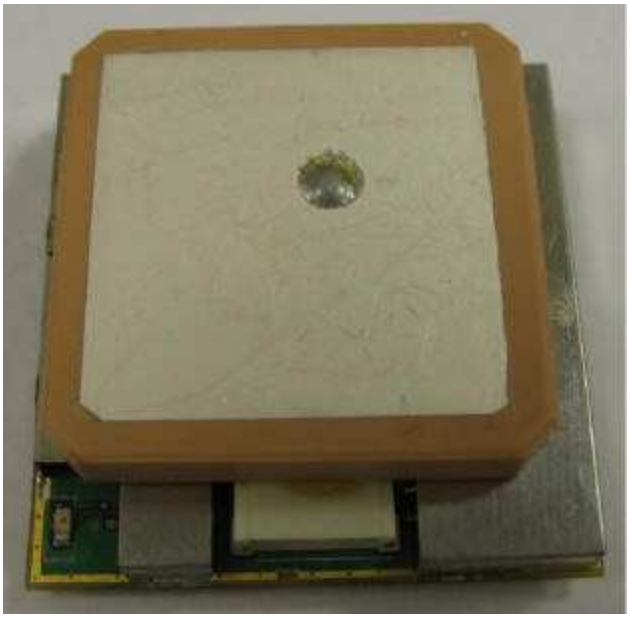
Protocol

Electrical level	TTL level, Output voltage level: 0V ~ 2.85V
	RS-232 level
Baud rate	4,800 bps
Output message	NMEA 0183 GGA, GSA, GSV, RMC, VTG, GLL

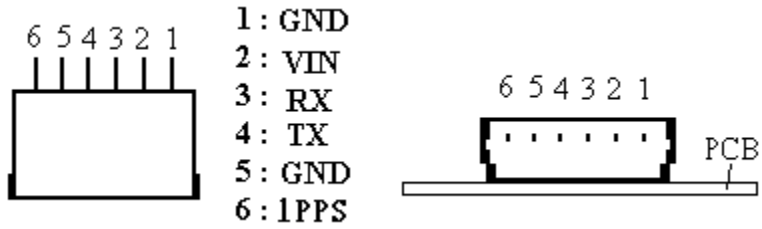
Physical Characteristics

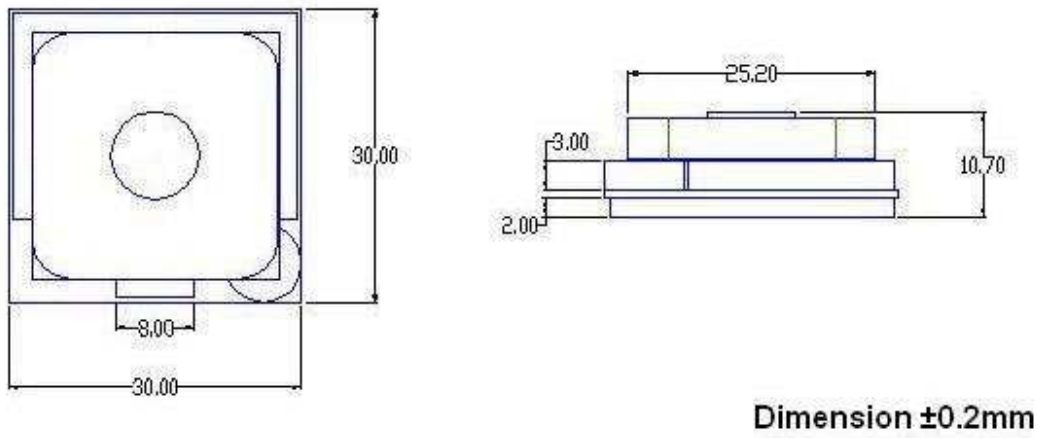
Dimension	30mm*30mm*10.5mm ¡Ó0.2mm

Operating temperature	-40¢J to +85¢J



Pin Assignment





Pin description

*** VIN (DC power input):**

This is the main DC supply for a 4.5V ~6.5 DC input power.

*** TX:**

This is the main transmits channel for outputting navigation and measurement data to user's navigation software or user written software.

*** RX:**

This is the main receive channel for receiving software commands to the engine board from SiRFdemo software or from user written software.

*** GND:**

GND provides the ground for the engine board. Connect all grounds.

*** 1PPS**

This pin provides one pulse-per-second output from the engine board that is synchronized to GPS time.

SOFTWARE COMMAND

NMEA Output Command

GGA-Global Positioning System Fixed Data

Table B-2 contains the values for the following example:

$GPGGA,161229.487,3723.2475,N,12158.3416,W,1,07,1.0,9.0,M,,,,0000*18

Table B-2 GGA Data Format

Name	Example	Units	Description
Message ID	$GPGGA		GGA protocol header
UTC Time	161229.487		hhmmss.sss
Latitude	3723.2475		ddmm.mmmm
N/S Indicator	N		N=north or S=south
Longitude	12158.3416		dddmm.mmmm
E/W Indicator	W		E=east or W=west
Position Fix Indicator	1		See Table B-3
Satellites Used	07		Range 0 to 12
HDOP	1.0		Horizontal Dilution of Precision
MSL Altitude[1]	9.0	meters	
Units	M	meters	
Geoid Separation[1]		meters	
Units	M	meters	
Age of Diff. Corr.		second	Null fields when DGPS is not used
Diff. Ref. Station ID	0000		
Checksum	*18		
<CR><LF>			End of message termination

SiRF Technology Inc. does not support geoid corrections. Values are WGS84 ellipsoid heights.

Table B-3 Position Fix Indicator

Value	Description
0	Fix not available or invalid
1	GPS SPS Mode, fix valid
2	Differential GPS, SPS Mode , fix valid
3	GPS PPS Mode, fix valid

GLL-Geographic Position-Latitude/Longitude

Table B-4 contains the values for the following example:

$GPGLL,3723.2475,N,12158.3416,W,161229.487,A*2C

Table B-4 GLL Data Format

Name	Example	Units	Description
Message ID	$GPGLL		GLL protocol header
Latitude	3723.2475		ddmm.mmmm
N/S Indicator	n		N=north or S=south
Longitude	12158.3416		dddmm.mmmm
E/W Indicator	W		E=east or W=west
UTC Position	161229.487		hhmmss.sss
Status	A		A=data valid or V=data not valid
Checksum	*2C		
<CR><LF>			End of message termination

GSA-GNSS DOP and Active Satellites

Table B-5 contains the values for the following example:

$GPGSA,A,3,07,02,26,27,09,04,15,,,,,,1.8,1.0,1.5*33

Table B-5 GSA Data Format

Name	Example	Units	Description
Message ID	$GPGSA		GSA protocol header
Mode1	A		See Table B-6
Mode2	3		See Table B-7
Satellite Used[1]	07		Sv on Channel 1
Satellite Used[1]	02		Sv on Channel 2
….			
Satellite Used[1]			Sv on Channel 12
PDOP	1.8		Position dilution of Precision
HDOP	1.0		Horizontal dilution of Precision
VDOP	1.5		Vertical dilution of Precision
Checksum	*33		
<CR><LF>			End of message termination

1. Satellite used in solution.

Table B-6 Mode1

Value	Description
M	Manual-forced to operate in 2D or 3D mode
A	2Dautomatic-allowed to automatically switch 2D/3D

Table B-7 Mode 2

Value	Description
1	Fix Not Available
2	2D
3	3D

GSV-GNSS Satellites in View

Table B-8 contains the values for the following example:

$GPGSV,2,1,07,07,79,048,42,02,51,062,43,26,36,256,42,27,27,138,42*71

$GPGSV,2,2,07,09,23,313,42,04,19,159,41,15,12,041,42*41

Table B-8 GSV Data Format

Name	Example		Description
Message ID	$GPGSV		GSV protocol header
Number of Messages[1]	2		Range 1 to 3
Message Number[1]	1		Range 1 to 3
Satellites in View	07		
Satellite ID	07		Channel 1(Range 1 to 32)
Elevation	79	degrees	Channel 1(Maximum90)
Azimuth	048	degrees	Channel 1(True, Range 0 to 359)
SNR(C/No)	42	dBHz	Range 0 to 99,null when not tracking
…..			…..
Satellite ID	27		Channel 4 (Range 1 to 32)
Elevation	27	Degrees	Channel 4(Maximum90)
Azimuth	138	Degrees	Channel 4(True, Range 0 to 359)
SNR(C/No)	42	dBHz	Range 0 to 99,null when not tracking
Checksum	*71		
<CR><LF>			End of message termination

Depending on the number of satellites tracked multiple messages of GSV data may be required.

RMC-Recommended Minimum Specific GNSS Data

Table B-10 contains the values for the following example:

$GPRMC,161229.487,A,3723.2475,N,12158.3416,W,0.13,309.62,120598,,*10

Table B-10 RMC Data Format

Name	Example	Units	Description
Message ID	$GPRMC		RMC protocol header
UTC Time	161229.487		hhmmss.sss
Status	A		A=data valid or V=data not valid
Latitude	3723.2475		ddmm.mmmm
N/S Indicator	N		N=north or S=south
Longitude	12158.3416		dddmm.mmmm
E/W Indicator	W		E=east or W=west
Speed Over Ground	0.13	knots	
Course Over Ground	309.62	degrees	True
Date	120598		ddmmyy
Magnetic Variation[2]		degrees	E=east or W=west
Checksum	*10		
<CR><LF>			End of message termination

SiRF Technology Inc. does not support magnetic declination. All “course over ground” data are geodetic WGS48 directions.

VTG-Course Over Ground and Ground Speed

$GPVTG,309.62,T,,M,0.13,N,0.2,K*6E

Name	Example	Units	Description
Message ID	$GPVTG		VTG protocol header
Course	309.62	degrees	Measured heading
Reference	T		True
Course		degrees	Measured heading
Reference	M		Magnetic
Speed	0.13	knots	Measured horizontal speed
Units	N		Knots
Speed	0.2	Km/hr	Measured horizontal speed
Units	K		Kilometers per hour
Checksum	*6E		
<CR><LF>			End of message termination

NMEA Input Command

A). Set Serial Port ID:100 Set PORTA parameters and protocol

This command message is used to set the protocol(SiRF Binary, NMEA, or USER1) and/or the communication parameters(baud, data bits, stop bits, parity). Generally,this command would be used to switch the module back to SiRF Binary protocol mode where a more extensive command message set is available. For example,to change navigation parameters. When a valid message is received,the parameters will be stored in battery backed SRAM and then the receiver will restart using the saved parameters.

Format:

$PSRF100,<protocol>,<baud>,<DataBits>,<StopBits>,<Parity>*CKSUM
<CR><LF>

<protocol>	0=SiRF Binary, 1=NMEA, 4=USER1
<baud>	1200, 2400, 4800, 9600, 19200, 38400
<DataBits>	8,7. Note that SiRF protocol is only valid f8 Data bits
<StopBits>	0,1
<Parity>	0=None, 1=Odd, 2=Even

Example 1: Switch to SiRF Binary protocol at 9600,8,N,1
$PSRF100,0,9600,8,1,0*0C<CR><LF>

Example 2: Switch to User1 protocol at 38400,8,N,1
$PSRF100,4,38400,8,1,0*38<CR><LF>

**Checksum Field: The absolute value calculated by exclusive-OR the 8 data bits of each character in the Sentence,between, but excluding "$" and "*". The hexadecimal value of the most significant and least significant 4 bits of the result are convertted to two ASCII characters (0-9,A-F) for transmission. The most significant character is transmitted first.

**<CR><LF> : Hex 0D 0A

B). Navigation lnitialization ID¡G101 Parameters required for start

This command is used to initialize the module for a warm start, by providing current position ¡] in X, Y, Z coordinates¡^,clock offset, and time. This enables the receiver to search for the correct satellite signals at the correct signal parameters. Correct initialization parameters will enable the receiver to acquire signals more quickly, and thus, produce a faster navigational solution.

When a valid Navigation Initialization command is received, the receiver will restart using the input parameters as a basis for satellite selection and acquisition.

Format¡G

$PSRF101,<X>,<Y>,<Z>,<ClkOffset>,<TimeOfWeek>,<WeekNo>,<chnlCount>,<ResetCfg>

*CKSUM<CR><LF>

<X>	X coordinate position INT32
<Y>	Y coordinate position INT32
<Z>	Z coordinate position INT32
<ClkOffset>	Clock offset of the receiver in Hz, Use 0 for last saved value if available. If this is unavailable, a default value of 75000 for GSP1, 95000 for GSP 1/LX will be used. INT32
<TimeOf Week>	GPS Time OfWeek UINT32
<WeekNo>	GPS Week Number UINT16 ¡] Week No and Time Of Week calculation from UTC time¡^
<chnlCount>	Number of channels to use.1-12. If your CPU throughput is not high enough, you

	could decrease needed throughput by reducing the number of active channels UBYTE
<ResetCfg>	bit mask 0×01=Data Valid warm/hotstarts=1 0×02=clear ephemeris warm start=1 0×04=clear memory. Cold start=1 UBYTE

Example: Start using known position and time.

¢CPSRF101,-2686700,-4304200,3851624,96000,497260,921,12,3*7F

C). Set DGPS Port ID:102 Set PORT B parameters for DGPS input

This command is used to control Serial Port B that is an input only serial port used to receive
RTCM differential corrections.
Differential receivers may output corrections using different communication parameters.
The default communication parameters for PORT B are 9600 Baud, 8data bits, 0 stop bits, and no parity.
If a DGPS receiver is used which has different communication parameters, use this command to allow the receiver to correctly decode the data. When a valid message is received, the parameters will be stored in battery backed SRAM and then the receiver will restart using the saved parameters.
Format:
¢CPSRF102,<Baud>,<DataBits>,<StopBits>,<Parity>*CKSUM<CR><LF>

<baud>	1200,2400,4800,9600,19200,38400
<DataBits>	8
<StopBits>	0,1
<Parity>	0=None,Odd=1,Even=2

Example: Set DGPS Port to be 9600,8,N,1

¢CPSRF102,9600,8,1.0*12

D). Query/Rate Control ID:103 Query standard NMEA message and/or set output rate

This command is used to control the output of standard NMEA message GGA, GLL, GSA, GSV RMC, VTG. Using this command message, standard NMEA message may be polled once, or setup for periodic output. Checksums may also be enabled or disabled depending on the needs of the receiving program. NMEA message settings are saved in battery backed memory for each entry when the message is accepted.

Format:

¢PSRF103,<msg>,<mode>,<rate>,<cksumEnable>*CKSUM<CR><LF>

<msg>

0=GGA,1=GLL,2=GSA,3=GSV,4=RMC,5=VTG

<mode> 0=SetRate,1=Query

<rate> Output every <rate>seconds, off=0,max=255

<cksumEnable> 0=disable Checksum,1=Enable checksum for specified message

Example 1: Query the GGA message with checksum enabled

¢PSRF103,00,01,00,01*25

Example 2: Enable VTG message for a 1Hz constant output with checksum enabled

¢PSRF103,05,00,01,01*20

Example 3: Disable VTG message

¢PSRF103,05,00,00,01*21

E). LLA Navigation lnitialization ID:104 Parameters required to start using Lat/Lon/Alt

This command is used to initialize the module for a warm start, by providing current position (in Latitude, Longitude, Altitude coordinates), clock offset, and time. This enables the receiver to search for the correct satellite signals at the correct signal parameters. Correct initialization parameters will enable the receiver to acquire signals more quickly, and thus, will produce a faster navigational soution.

When a valid LLANavigationInitialization command is received,the receiver will restart using the input parameters as a basis for satellite selection and acquisition.

Format:

¢CPSRF104,<Lat>,<Lon>,<Alt>,<ClkOffset>,<TimeOfWeek>,<WeekNo>, <ChannelCount>, <ResetCfg>*CKSUM<CR><LF>

<Lat> Latitude position, assumed positive north of equator and negative south of equator float, possibly signed

<Lon> Longitude position, it is assumed positive east of Greenwich and negative west of Greenwich
Float, possibly signed

<Alt> Altitude position
float, possibly signed

<ClkOffset> Clock Offset of the receiver in Hz, use 0 for last saved value if available. If this is unavailable, a default value of 75000 for GSP1, 95000 for GSP1/LX will be used.
INT32

<TimeOfWeek> GPS Time Of Week
UINT32

<WeekNo> GPS Week Number
UINT16

<ChannelCount> Number of channels to use. 1-12
UBYTE

<ResetCfg>	bit mask	0×01=Data Valid warm/hot starts=1 0×02=clear ephemeris warm start=1 0×04=clear memory. Cold start=1 UBYTE

Example: Start using known position and time.

¢CPSRF104,37.3875111,-121.97232,0,96000,237759,922,12,3*37

F). Development Data On/Off ID:105 Switch Development Data Messages On/Off

Use this command to enable development debug information if you are having trouble getting commands accepted. Invalid commands will generate debug information that should enable the user to determine the source of the command rejection. Common reasons for input command rejection are invalid checksum or parameter out of specified range. This setting is not preserved across a module reset.

Format: ¢CPSRF105,<debug>*CKSUM<CR><LF>

<debug>	0=Off,1=On

Example: Debug On ¢CPSRF105,1*3E

Example: Debug Off ¢CPSRF105,0*3F

G). Select Datum ID:106 Selection of datum to be used for coordinate Transformations

GPS receivers perform initial position and velocity calculations using an earth-centered earth-fixed (ECEF) coordinate system. Results may be converted to an earth model (geoid) defined by the selected datum. The default datum is WGS 84 (World Geodetic System 1984) which provides a worldwide common grid system that may be translated into local coordinate systems or map datums. (Local map datums are a best fit to the local shape of the earth and not valid worldwide.)

Examples:

Datum select TOKYO_MEAN

$PSRF106,178*32

Name	Example	Units	Description
Message ID	$PSRF106		PSRF106 protocol header
Datum	178		21=WGS84 178=TOKYO_MEAN 179=TOKYO_JAPAN 180=TOKYO_KOREA 181=TOKYO_OKINAWA
Checksum	*32		
<CR> <LF>			End of message termination

Bibliographie

Vous trouverez dans cette section les références de quelques ouvrages qui m'ont servi durant la rédaction de ce polycopié.

A. Tanenbaum, "*Architecture de l'ordinateur*", 4eme édition, 1999, Editions Dunod.

Une référence, décrit l'ordinateur suivant une décomposition en couches qui vont des portes logiques jusqu'au programme en passant par le processeur et les OS. Dans le cadre du cours, on s'attardera plus précisément sur la couche physique, présentée au chapitre 3 ainsi que la description des OS donnée au chapitre 6.

D.-A. Patterson and J.-L. Hennessy, "*Computer Organization and Design, The Hardware/Software interface*", 2nd Edition, 1997, Editions Morgan Kaufmann.

Une bible de la conception, à l'instar du Tanenbaum. Il est plus focalisé sur les aspects quantitatifs (analyses performance/coût). Le chapitre 6 traite plus particulièrement de l'interfaçage.

W. Wolf, "*Computers as Components*", 2001, Editions Morgan Kaufman.

Un bon guide pour la conception des systèmes embarqués. Présente un ensemble d'outils pour le concepteur. On s'intéressera aux chapitres 3 et 5, traitant de l'interfaçage.

F. Dubos, "*Microprocesseur 68020, conception et applications*", 1991, Editions Masson.

Un exemple de processeur. Le 68020 n'est plus vraiment utilisé actuellement. Il vaut mieux privilégier l'étude, soit d'un processeur actuel (PowerPC, ARM, Pentium) soit d'un processeur didactique ou une architecture de référence (68000, 8088).

M. Baar, "*Programming Embedded Systems in C and C++*", 1999, Editions O'Reilly.

Décrit les outils nécessaires au développement des systèmes embarqués, du point de vue du développeur logiciel. Court (moins de 200p) et précis.