3DMIA: A Multi-objective Artificial Immune Algorithm for 3D-MPSoC Multi-Application 3D-NoC Mapping

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ABSTRACT
Three dimensional Multiprocessor System-on-Chip (3D-MPSoC) are characterized by the integration of a large amount of hardware components targeting a wide range of application on a single chip. However, heating is one of the major pitfalls of the 3D-MPSoCs. Three dimensional Network-on-Chip (3D-NoC) is used as the communication structure of the 3D-MPSoC. Its main role in the system operation and performance turns critical the optimal 3D-NoC design. Mapping is one of the most critical 3D-NoC parameters, strongly influencing the 3D-MPSoC performance. In this paper we propose the use of a multi-objective immune algorithm (3DMIA), *an evolutionary approach* to solve the multi-application 3D-NoC mapping problem. Latency and power consumption were adopted as the target multi-objective functions constrained by the heating function. Final 3D-NoC configurations enhance up to 73% the power and 42% the latency when compared to the previous reported results. We also evaluate the effect on the mutation rate and population size on the convergence speed of 3DMIA. We find that the adaptive mutation rate increases the performance of 3DMIA up to 84% when compared to static mutation rate approach.

Categories and Subject Descriptors
J [**Computer applications**]

General Terms
Algorithms, Performance, Design.

1. INTRODUCTION
3D-MPSoC integrates vertically multiple programmable processor cores, specialized memories and other intellectual property (IP) components into different dies (layers) stacked on a single chip. 3D-MPSoC brings as its major advantage the capability of supporting many applications on a single chip (multi-application system) [1,2]. Each application is characterized by a set of performance requirements. Applications can be mapped dynamically on the 3D-MPSoC. Therefore, there is no a single and static performance requirement, but a set of ever changing performance requirements that must be satisfied. However, vertical integration of layers exacerbates the thermal problems. Heating is one of the major pitfalls of the 3D-MPSoCs. A 3D-MPSoC must support numerous concurrent tasks, each one characterized by distinct power and thermal characteristics.

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Managing heterogeneous workloads to optimize performance and temperature is challenging. Hotspots due to the overloading of tasks execution on some 3D-MPSoCs areas can cause the malfunction of the system. 3D-NoCs are employed as the communication structure of the 3D-MPSoCs [4-7]. It links vertically several 2D-NoCs by means of Through-Silicon-Vias (TSV). Finding an optimal 3D-NoC configuration to meet all the communication requirements of all the applications supported by the 3D-MPSoC is not an easy task [2]. The *mapping problem* deals with the allocation of the IP cores onto the network routers. Final solution must satisfy all the application requirements, consisting of multiple desired objectives that are frequently in contrast with each other [2]. According to [1], 3D-NoC mapping is one of the most critical steps in 3D-NoC design. Mapping is a quadratic assignment problem that is known to be NP-hard [3]. The best mapping solutions have been obtained using a multi-objective strategy [3]. As a result, the designer obtains a set of best mapping alternatives (*Pareto optimal set*) featuring different trade-offs among the performance indexes [4-6]. In this work we propose 3DMIA, a Multi-objective Adaptive Immune Algorithm to solve the multi-application 3D-NoC mapping problem with the purpose of reducing the latency and power under heating constraints. 3DMIA performs the mapping search using static evaluation (analytical model). It determines the best 3D-NoC mappings which are then simulated through a SystemC-TLM 3D-NoC evaluation framework [4]. The simulation performs the dynamic evaluation of the mapping alternatives under different traffic conditions. We compared our solution with previous reported genetic (3D-RMGA) approach [3]. Our work presents 3 novelties: i) the use of a multi-objective immune algorithm to solve the 3D-NoC mapping problem under contrasting objectives (power and latency); ii) the solution of the 3D-NoC mapping problem for multi-application systems; and iii) the consideration of heating constraints. The remaining text is divided into 5 sections. Section 2 presents an overview of the previous 3D multi-objective mapping works. Section 3 presents the 3DMIA mapping algorithm. Section 4 shows our experimental results and the comparison among GA and SA. Finally we present our conclusions in Section 5.

2. RELATED WORKS
Only [3], has proposed a multi-objective 3D-NoC mapping based on a rank-based genetic algorithm (RMGA) with the purpose of reducing the latency under congestion and the latency under non-congestion (agreeing objectives). However, heating issues of the 3D-MPSoC is not taken into account. It codifies the different mapping alternatives in chromosomes. The mapping alternatives are evaluated through an analytical model (static model).

3. 3DMIA DESCRIPTION

In order to solve the multi-application 3D-MPSoC mapping, 3DMIA adopts the combination of the APCGs of the applications executed on the 3D-MPSoC. A synthetic APCG is generated and used as an entry of the optimization process. The new APCG is called Worst-Case APCG (W-APCG). It includes all 3D-MPSoC IP cores and all the requirements of the applications that are being mapped on the system. For the communication flow between every pair of IP cores, the tightest communication requirements across all the applications are selected as the requirements of the W-APCG. 3DMIA is an extension of MAIA presented in [5].

Fig 1 shows the algorithm flow of 3DMIA. It is composed of six phases. Fig 2 shows the antibody representation. 3DMIA uses an analytical 3D-NoC model built from the queuing theory. The objective functions and 3DMIA parameters are summarized in Table I.

Setting 3DMIA control parameters: Mutation rate μ_r is considered one of the most sensitive parameters for the immune algorithms. It increases the diversity in the population, so as to prevent getting stuck at a local optimal value during the optimization search. 3DMIA uses an adaptive mutation rate, which varies according to the fitness value of the mapping alternatives. μ_r has a lower value for high fitness mappings and higher value for lower fitness mappings. The high fitness mappings aid the convergence of 3DMIA, while low fitness mappings prevent that 3DMIA gets stuck at a local optimum.

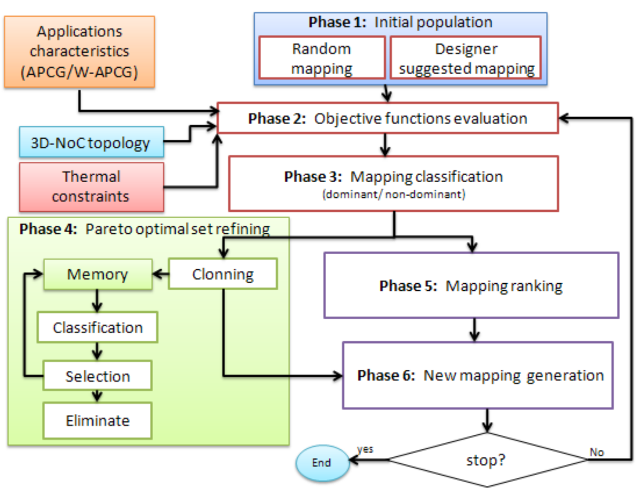

Figure 1. 3DMIA algorithm.

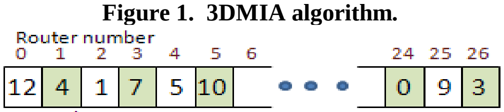

Figure 2. Mapping alternative (antibodies) representation.

Table 1. 3DMIA parameters

Parameter	*Value*
Initial population M (phase 2)	100 - 200
Latency objective function	$L_{3DNoC\ [2]}$
Power objective function	$P_{3DNoC\ [2]}$
Heating Constraint	$H_{3DNoC\ [1]}$
Dynamic mutation rate (phase5)	[0.02, 0.05]
Crossover (phase7)	40%
Stop criterion	0.1

4. EXPERIMENTAL WORK

3DMIA was tested and compared with the multi-objective rank-based genetic algorithm (3D-RMGA) [9]. We implemented both algorithms in C++. For comparison purposes, the two algorithms use the same analytical model L_{3DNoC}, P_{3DNoC} e H_{3DNoC}. We tested 8 benchmarks that integrates up to 243 IPs an up to 8 applications in a single chip. APCGs values of each benchmark were randomly selected. 3DMIA finds 3D-NoC mappings that decrease the power consumption and latency in average 37% and 58% respectively over 3D-RMGA. Moreover, when the simulation of the Pareto set was performed, the total values of the latency increase up to 30%. However, the 3DMIA solutions outperform the Pareto set of 3D-RMGA up to 45% and 37%. We evaluate the sensibility of 3DMIA with respect to the mutation rate μ_r in terms of the number of generations required to find the Pareto optimal set. μ_r was varied from 0.01 to 1. Each point of the Fig 3 was evaluated by taking the average of 100 independent runs of 3DMIA. The population size was fixed to 200. We observe that the performance of MAIA depends on the characteristics of the benchmark. However, we observe that the best performances of 3DMIA are achieved for μ_r that varies in the interval [0.02, 0.1]. By using a dynamic mutation rate, the performance of 3DMIA was improved up to 84% compared to the 3DMIA static mutation rate and 215% to the 3D-RMGA approach.

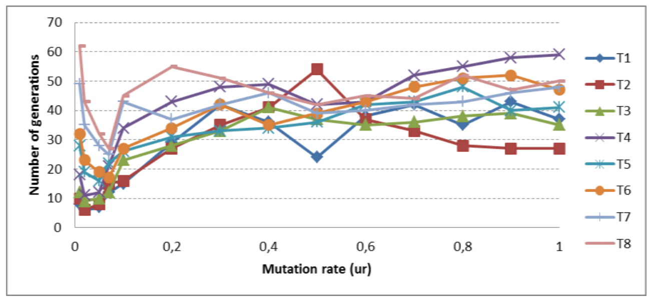

Figure 3. Impact of mutation rate over 3DMIA.

5. CONCLUSION

3DMIA is an efficient approach that performs an efficient exploration of the huge search space of the 3D-NoC mapping problem. It finds 3D-NoC solutions with contrast performance objectives. However, the Pareto-optimal set must always be evaluated under dynamic conditions (simulation), once the dynamic behavior is difficult to predict. The tuning of mutation rate allows that 3DMIA outperforms previous GA solutions up to 215%. As a future work, we plan to explore the population size parameter in order to improve even more 3DMIA.

6. REFERENCES

[1] Aggarwal A., Kumar S., Zjajo A., Leuken R.: Temperature Constrained Power management Scheme for 3D MPSoC. In Proc. IEEE 16th Workshop on Signal and power integrity (SPI 2012).

[2] Sheibanyrad, A. et al, "3D integration for NoC-based SoC Architectures". Integrated Circuits and Systems. Springer. 2011

[3] Wang J., Li L., Pan H., He S., Zhang R.: Latency aware mapping for 3D NoC using ra-based multi-objective genetic algorithm. In Proc. ASICON 2011.

[4] Sepulveda J., Pedraza C., Gogniat G., Pires R. Wang C., Strum M.: QoS 3D-HoC Hybrid-on-Chip Communication Structure for dynamic 3D-MPSoC. LASCAS 2013.

[5] Sepulveda J., Gogniat G., Pires R. Wang C., Strum M.: A multi-objective approach for Multi-application NoC mapping. LASCAS 2011.