

7th International Symposium on Turbo Codes & Iterative Information Process
ISTC 2012, Gothenburg, Sweden, 27-31 Aug, 2012

A Space-Time Redundancy Technique for Embedded Stochastic Error Correction

- A Decoder Against Internal Faults

A Collaborative Work of



LEFT Lab:

Utah State University, Utah, USA

Dr. Chris Winstead



Lab-STICC:

Université de Bretagne Sud, France

Pr. Emmanuel Boutillon, Presenter: Yangyang Tang

Email: yangyang.tang@univ-ubs.fr



Institut Polytechnique Bordeaux, France

Pr. Christophe Jégo



TELECOM Bretagne, France

Pr. Michel Jézéquel

OUTLINE

1. Emerging Challenge in Electronic Device

2. Previous Work: Coded Dual-Modular Redundancy (cDMR)

3. Latest Solution: A Decoder Against Internal Faults

4. Space-Time Redundancy Technique

5. Conclusions & Discussions

OUTLINE

1. Emerging Challenge in Electronic Device

2. Previous Work: Coded Dual-Modular Redundancy (cDMR)

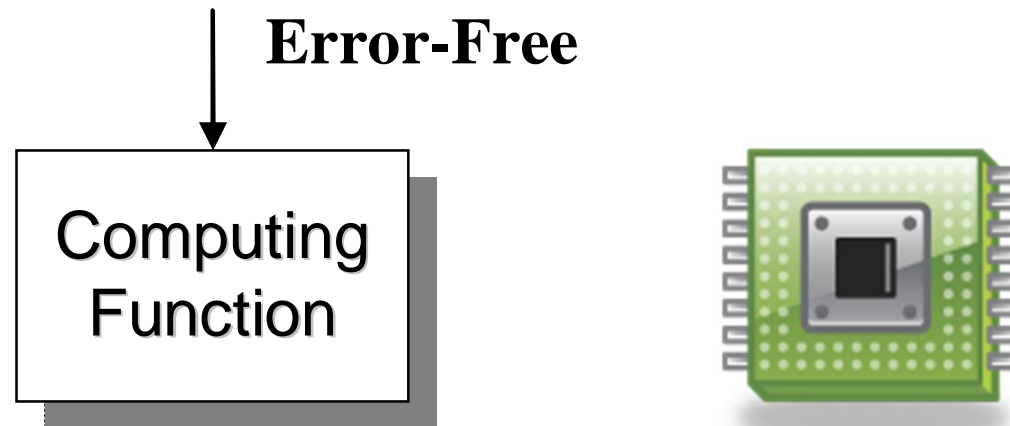
3. Latest Solution: A Decoder Against Internal Faults

4. Space-Time Redundancy Technique

5. Conclusions & Discussions

Electronic Device: Phase 1 Æ Error Free

“ Phase 1: Reliable, Computation is Error-Free.



Emerging Challenge: Transient Fault Sources

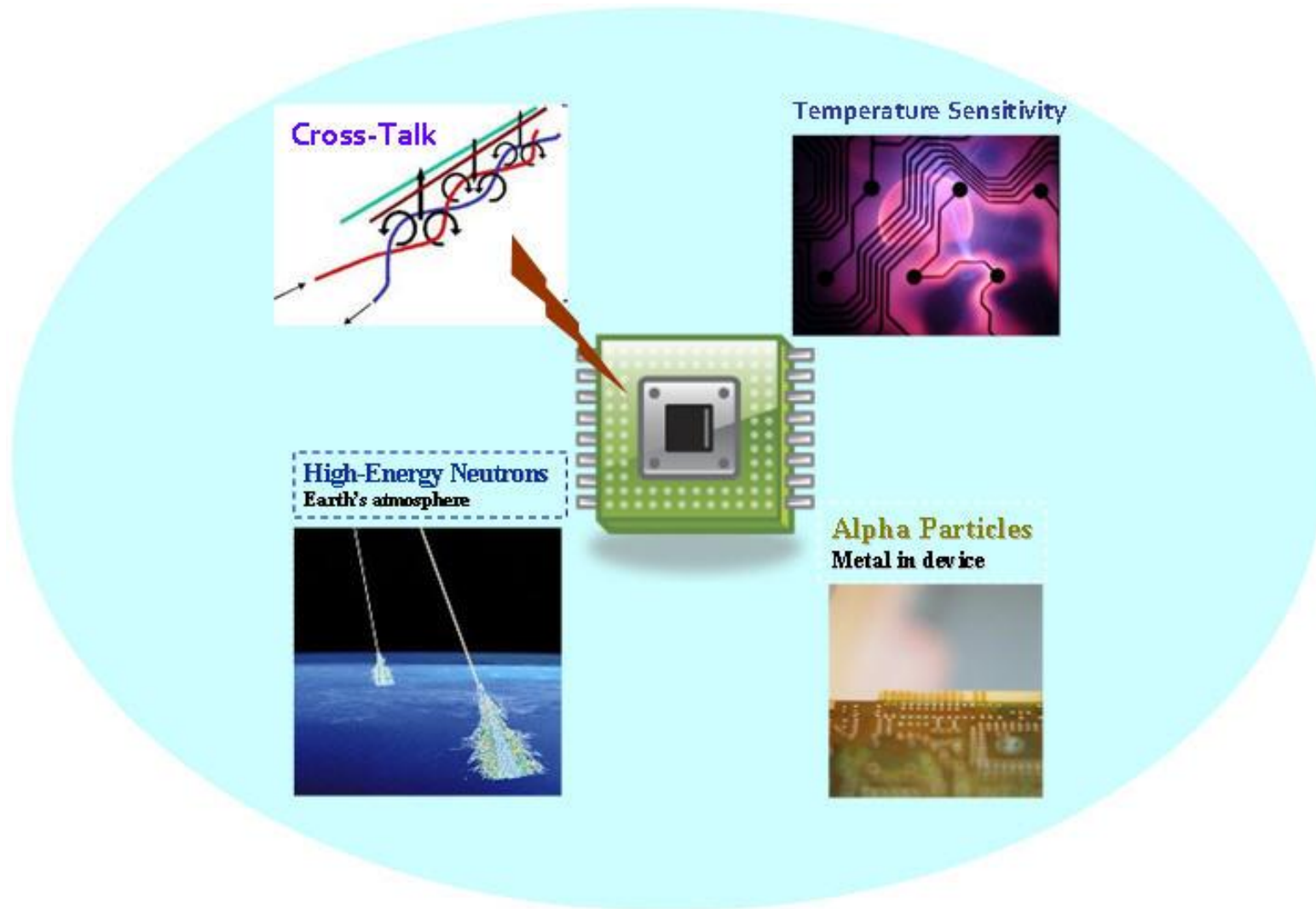
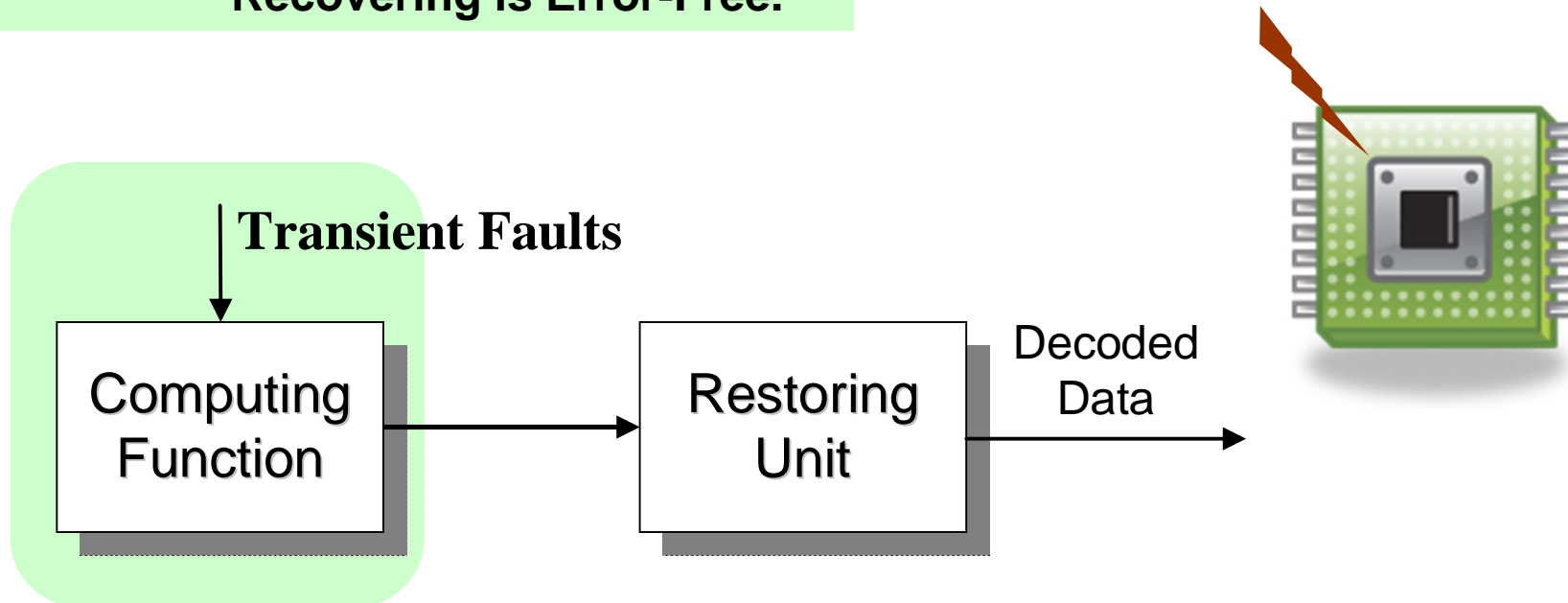


Fig. 1: Transient Fault Sources: Cross-Talk, Thermal, Soft-Error: by High-Energy Neutron and Alpha Particles, and etc

Electronic Device: Phase 2 – Recovering is Error-Free

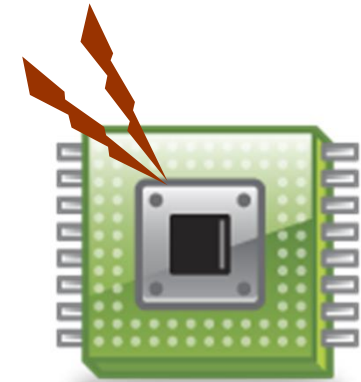
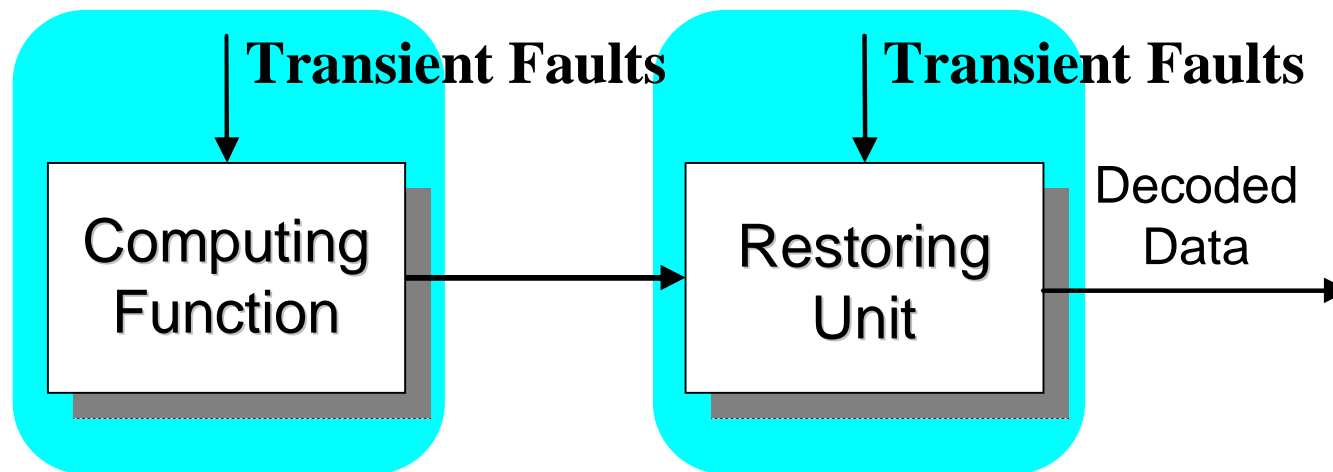
” Phase 2: Computation is Erroneous,
Recovering is Error-Free.



Unreliable Function & Unreliable Restoration

“ Phase 3: Computation is Erroneous,
Recovering is Erroneous as well.

*Sample: Y. Tang, E. Boutillon, M.
Jézéquel, C. Jégo, 2011*



OUTLINE

1. Emerging Challenge in Electronic Device

2. Previous Work: Coded Dual-Modular Redundancy (cDMR)

3. Latest Solution: A Decoder Against Internal Faults

4. Space-Time Redundancy Technique

5. Conclusions & Discussions

Coded Dual Modular-Redundancy (cDMR)

Sample of C. Winstead's work in 2009 and also our work at ISCAS 2012.

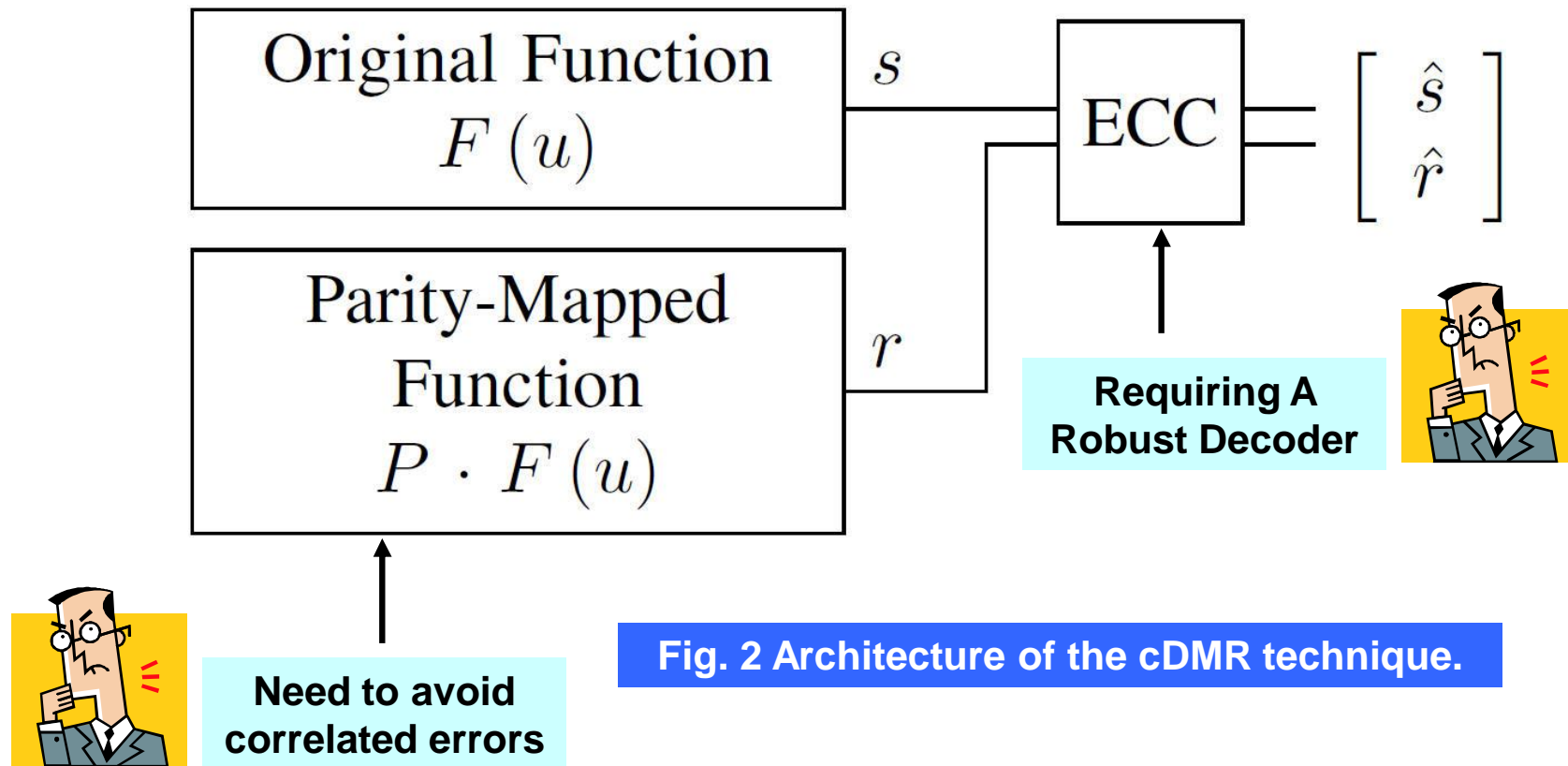
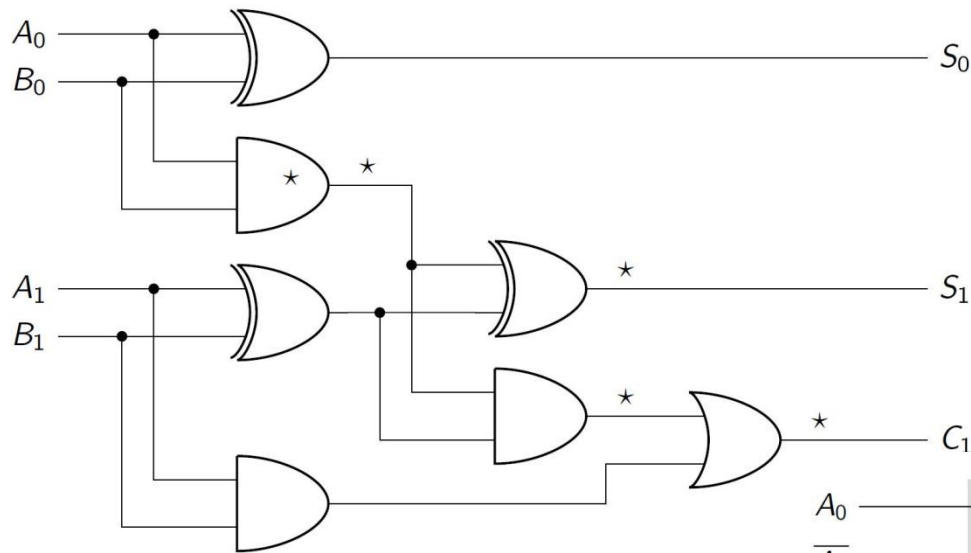


Fig. 2 Architecture of the cDMR technique.

“The original logic function $F(u)$ is composed with a block ECC code to create the parity-mapped function $P \cdot F(u)$.”

Parity-Mapped Function

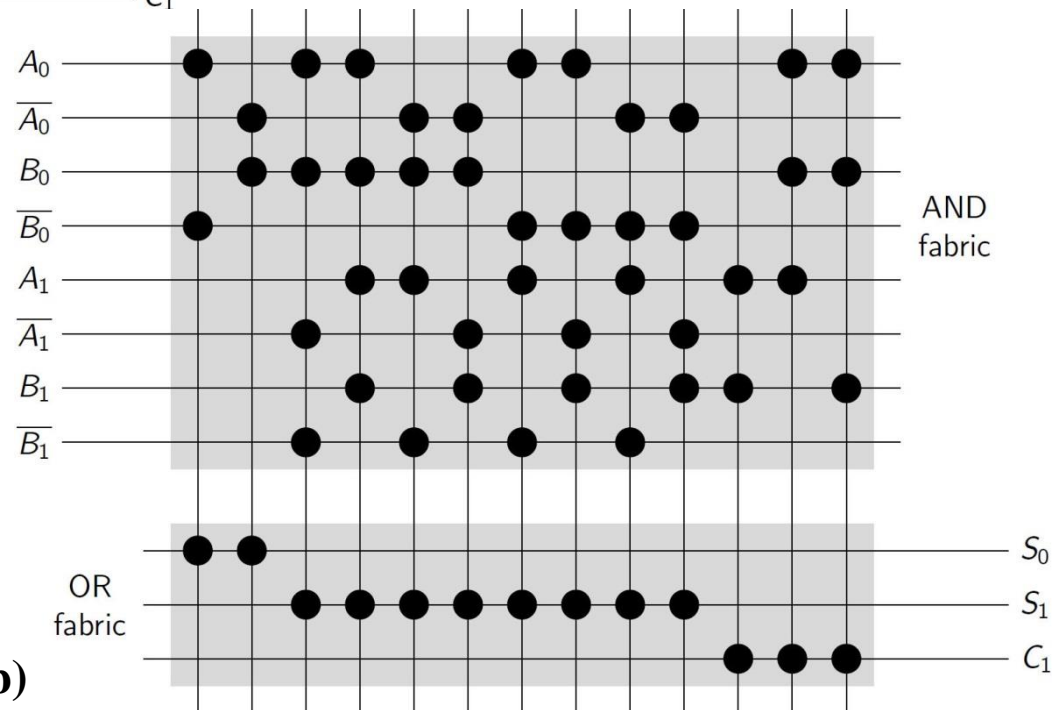
Sample of our work at ULSI
2012.



(a)

Fig. 3 (a) Traditional ripple-carry design, * symbol indicates the occurrence of an error.

An approach to built Parity-Mapped Function without correlated error occurrence.



(b)

Fig. 3 (b) Crossbar design suitable for some nanoelectronic device families.

Decoder for Binary Symmetric Channel

Ref: Gallager-A decoding Method, R. Gallager, 1963.

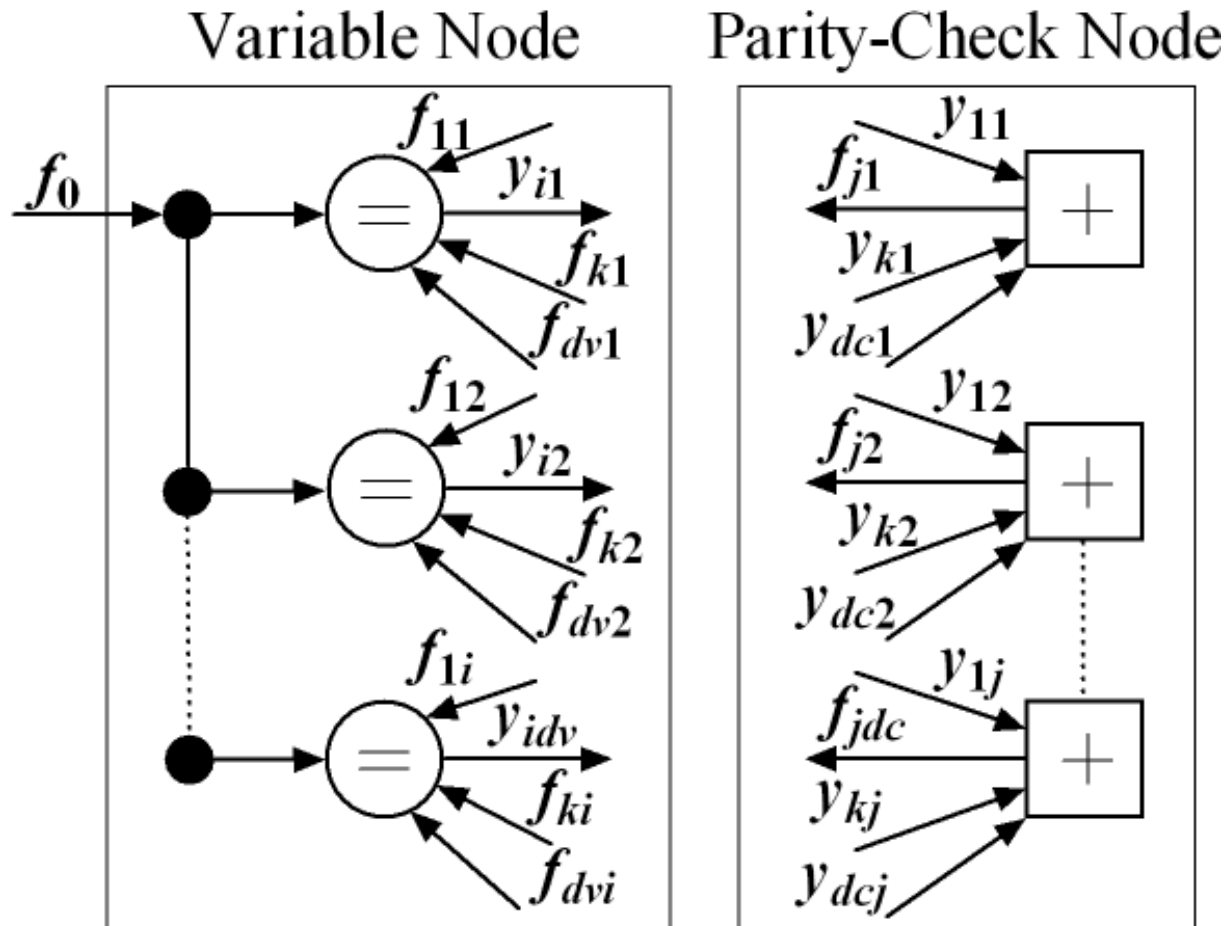


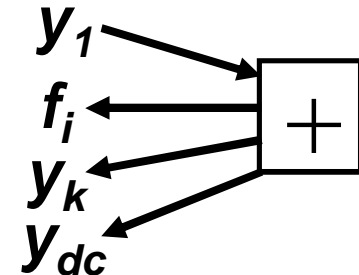
Fig. 4 Message-Passing Decoding Variable-Node & Check-Node

Ref: message-passing decoding, T. Richardson and R. Urbanke, 2001.

Gallager-A Decoder

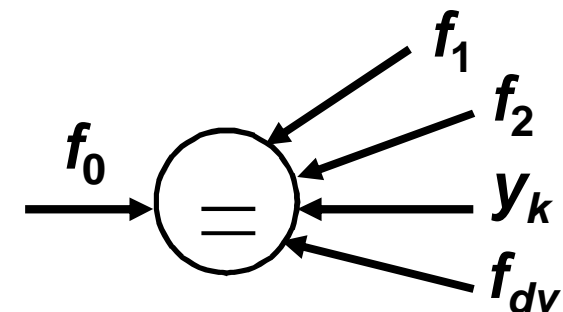
Check Node Processing

$$f_i = \bigoplus_{k \in \mathcal{C}_i} y_k$$



Variable Node Processing

$y_k = f_0$ if $(f_i, i \in \mathcal{C}_k)$ disagree, f_1 otherwise



OUTLINE

1. Emerging Challenge in Electronic Device

2. Previous Work: Coded Dual-Modular Redundancy (cDMR)

3. Latest Solution: A Decoder Against Internal Faults

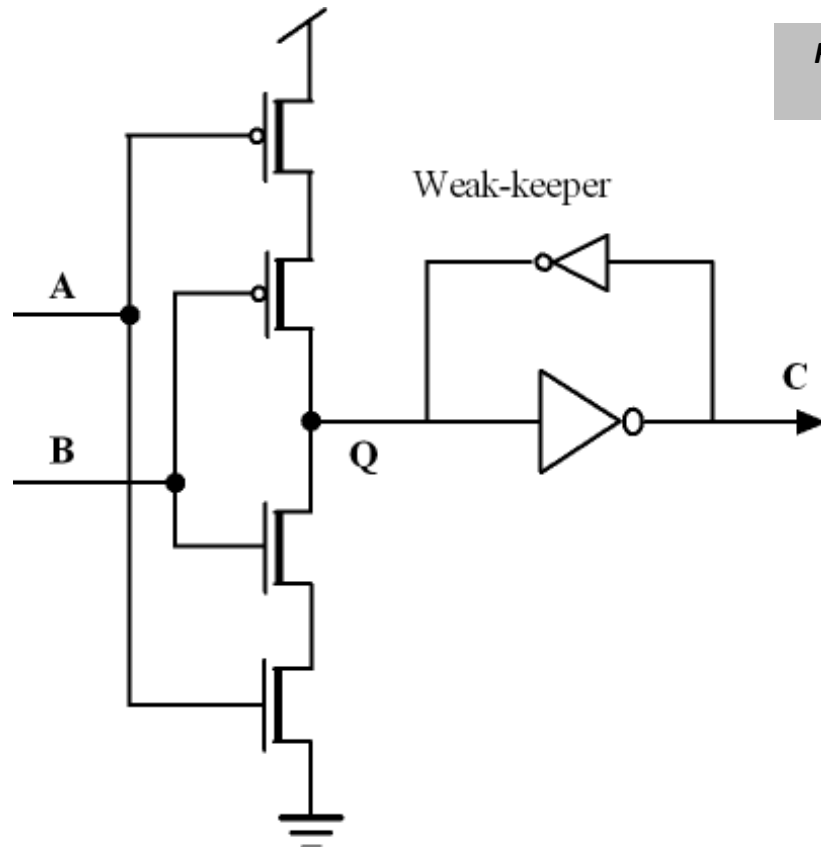
4. Space-Time Redundancy Technique

5. Conclusions & Discussions

Muller C-element: *Error-Resilience in Nature*

Ref : D. E. Muller and W. S. Bertky, 1959

C-element



Tab. 1 Truth-Table of Binary C-element

A	B	C
0	0	0
0	1	C_{n-1}
1	0	C_{n-1}
1	1	1

" C_{n-1} denotes the state maintained via weak feedback.

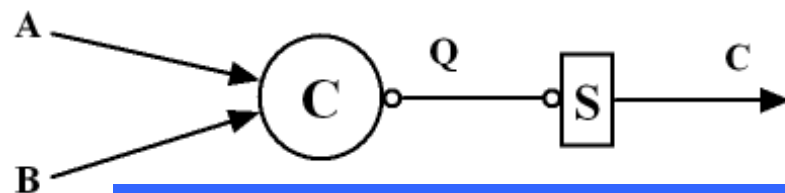
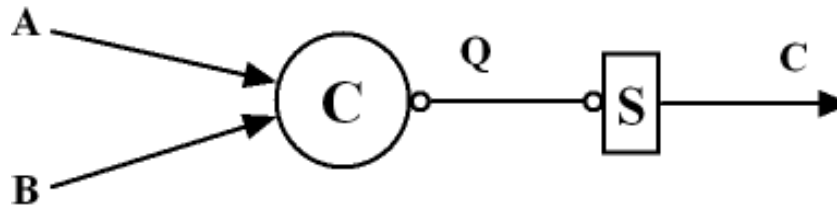


Fig. 5 CMOS Implementations of binary C-element

Muller C-element: *Error-Resilience in Nature*

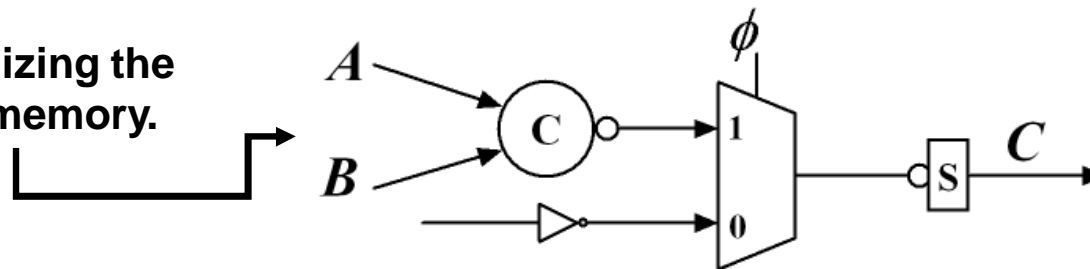
C-element



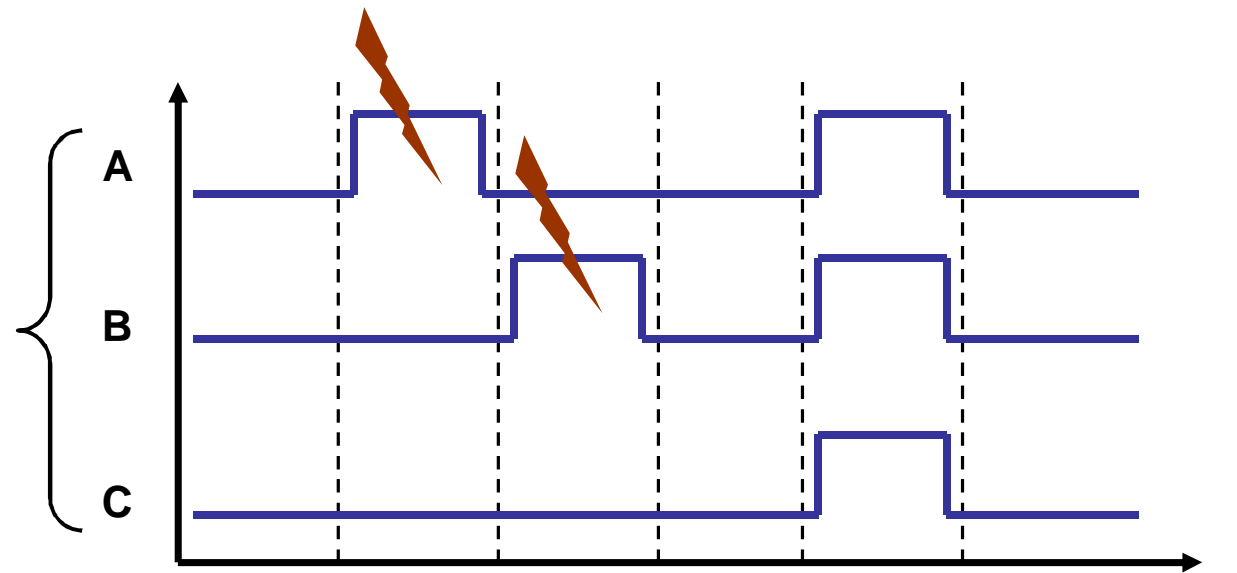
Tab. 1 Truth-Table of Binary C-element

A	B	C
0	0	0
0	1	C_{n-1}
1	0	C_{n-1}
1	1	1

" Initializing the state memory.



Error-Resilience in Nature



LDPC Stochastic Decoding Method (LSD)

Sample of our work 2012 at
ISCAS 2012.

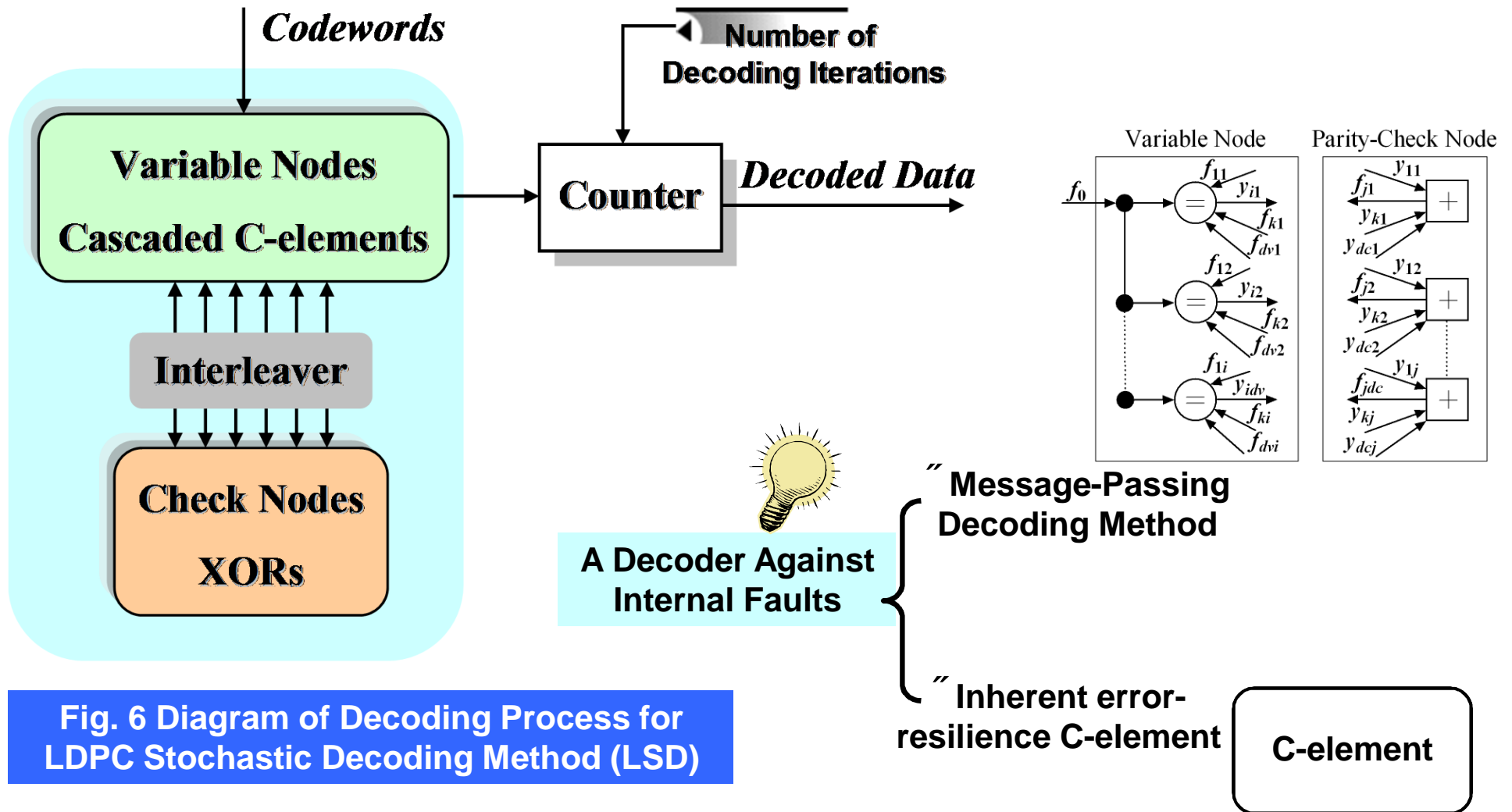
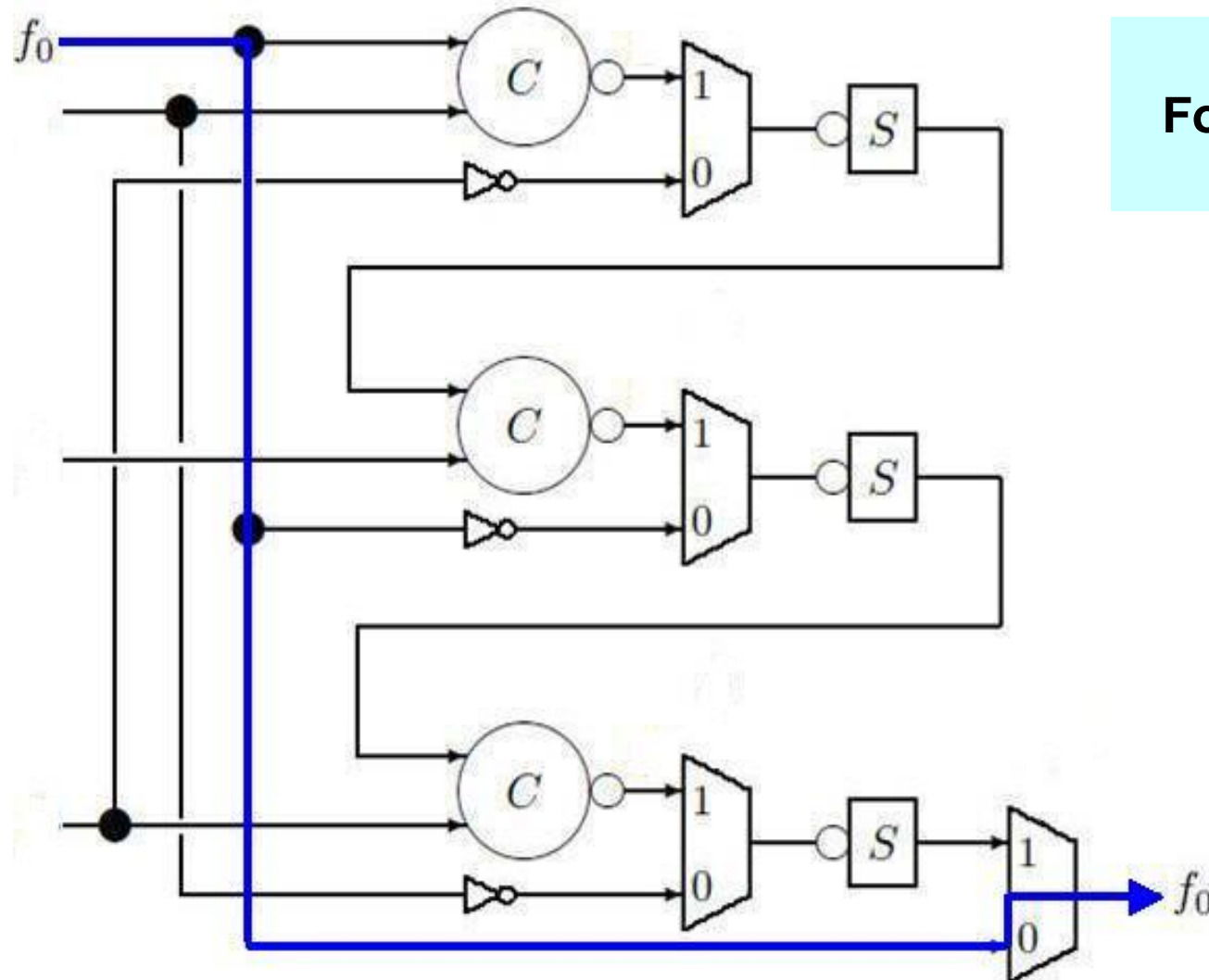


Fig. 6 Diagram of Decoding Process for LDPC Stochastic Decoding Method (LSD)

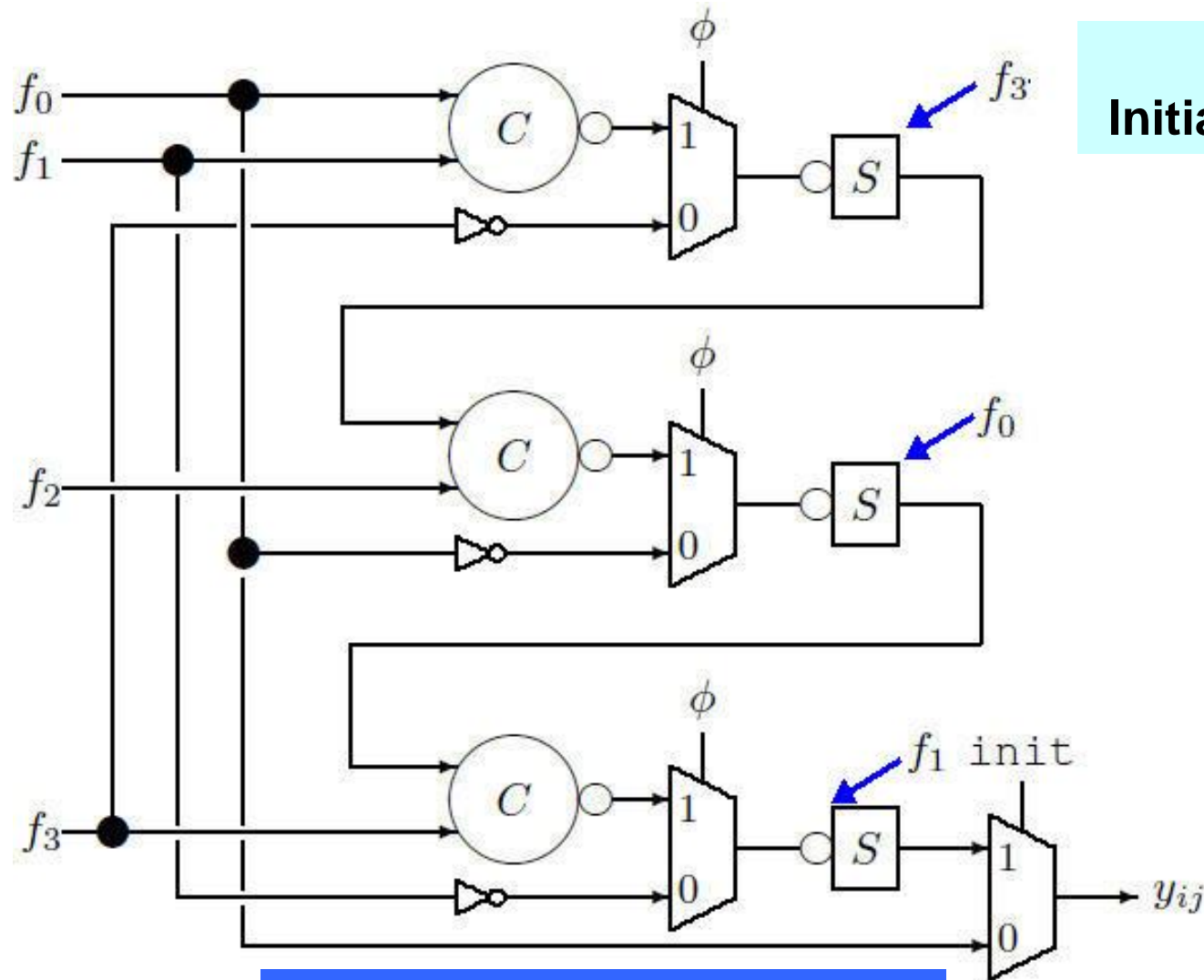
Variable Node in LSD \ddot{E} Phase 0



**Phase 0
Forward Channel
Message**

**Fig. 7 Basic Error-Correction
Unit Cascaded C-elements, $d_v=4$**

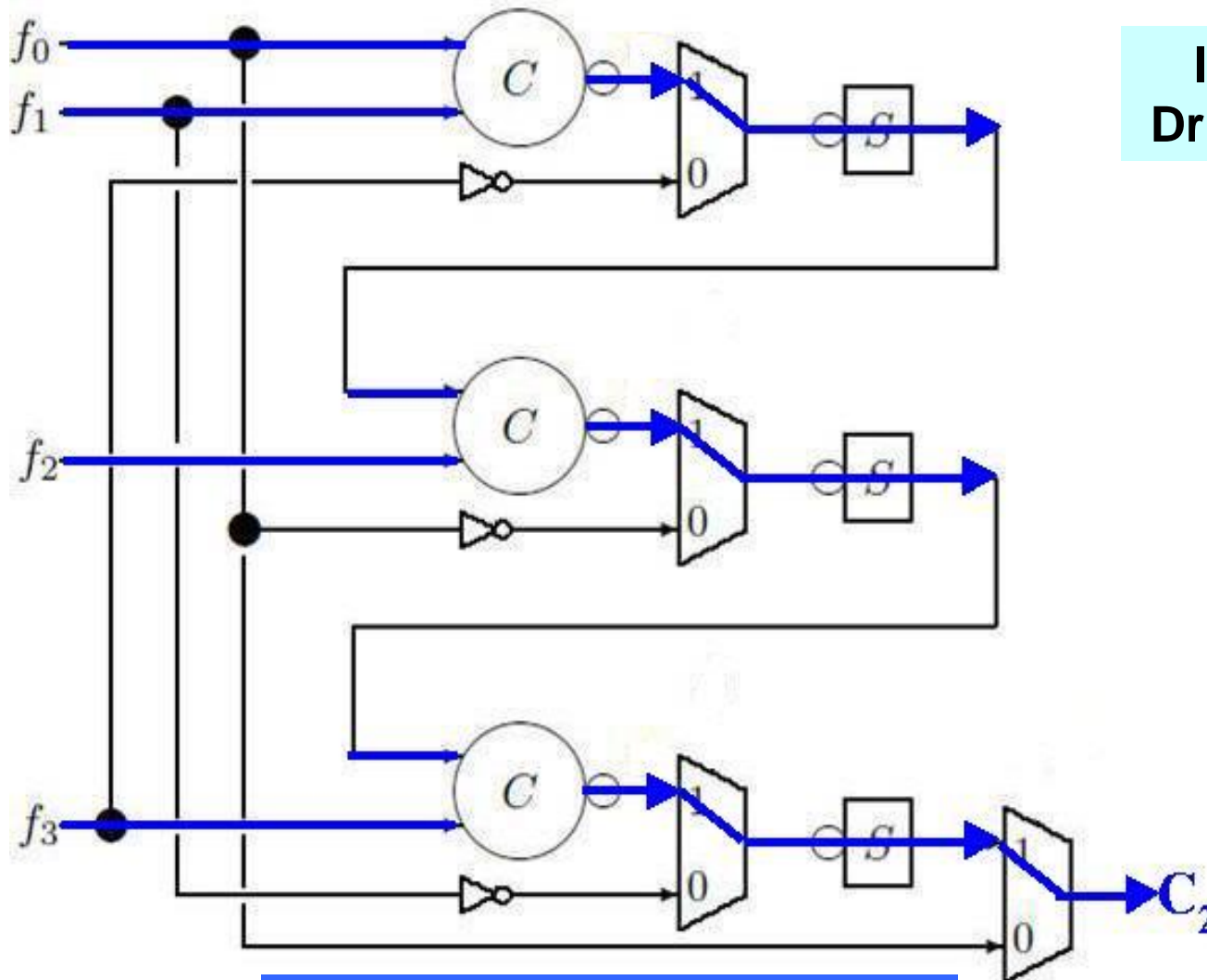
Variable Node in LSD \ddot{E} Phase 1



**Phase 1
Initialization Phase**

**Fig. 7 Basic Error-Correction
Unit Cascaded C-elements, $d_v=4$**

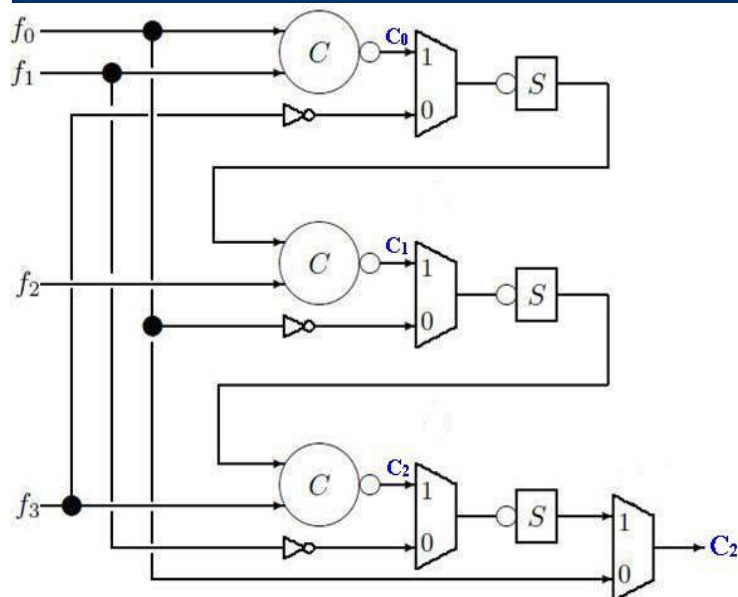
Variable Node in LSD \ddot{E} Phase 2



Iterative Phase 2
Driven by C-element

Fig. 7 Basic Error-Correction Unit Cascaded C-elements, $d_v=4$

Variable Node in LSD



Variable Nodes
Cascaded C-elements

Cascaded C-element is able to correct a single error during one iteration

Tab. 2 A truth table that illustrates the behaviors of error-correction

					Initialization			In 1 Iteration		
	f_0	f_1	f_2	f_3	C_0	C_1	C_2	C_0	C_1	C_2
Error-Free	0	0	0	0	0	0	0	0	0	0
Error in f_0	1	0	0	0	0	1	0	0	0	0
Error in f_1	0	1	0	0	0	0	1	0	0	0
Error in f_2	0	0	1	0	0	0	0	0	0	0
Error in f_3	0	0	0	1	1	0	0	0	0	0

OUTLINE

1. Emerging Challenge in Electronic Device

2. Previous Work: Coded Dual-Modular Redundancy (cDMR)

3. Latest Solution: A Decoder Against Internal Faults

4. Space-Time Redundancy Technique

5. Conclusions & Discussions

A Modified LSD (LSDfb): Feedback Mechanism

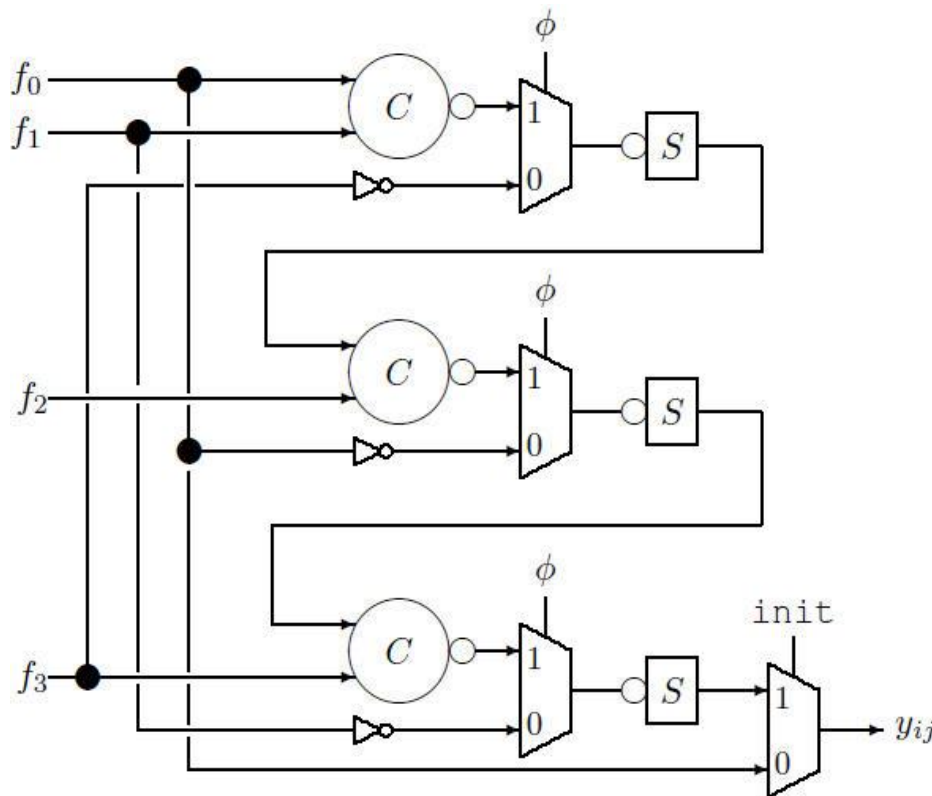


Fig. 7 LSDB variable-node architecture, $d_v=4$

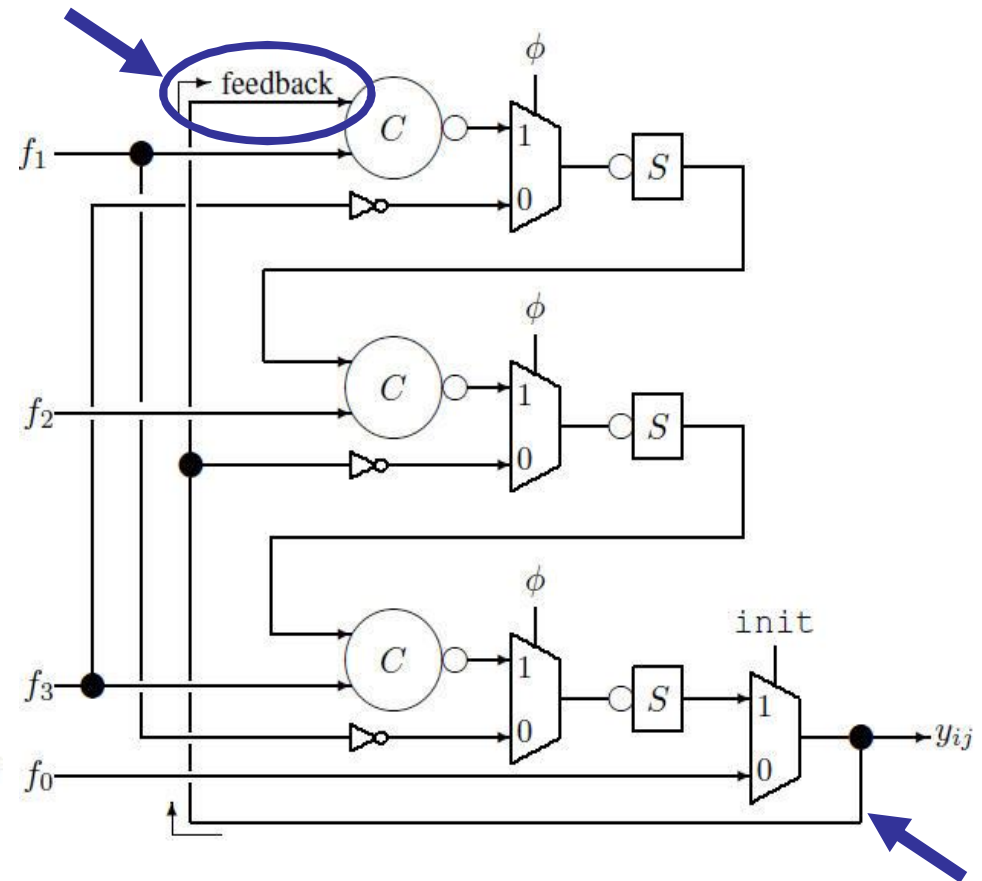


Fig. 8 LSDfb variable-node architecture, $d_v=4$

A Contribution of this work : A feedback mechanism employed to suppress internal fault event.

Space-Time Redundancy Technique

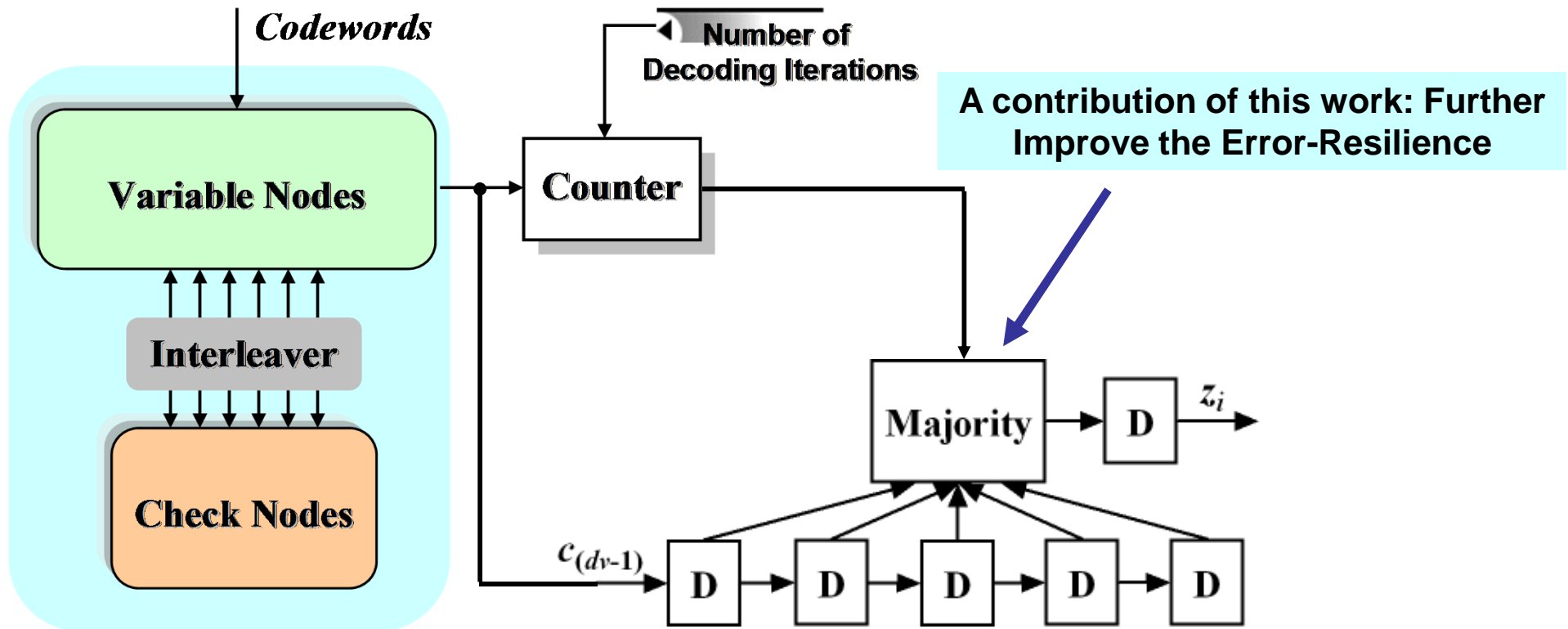
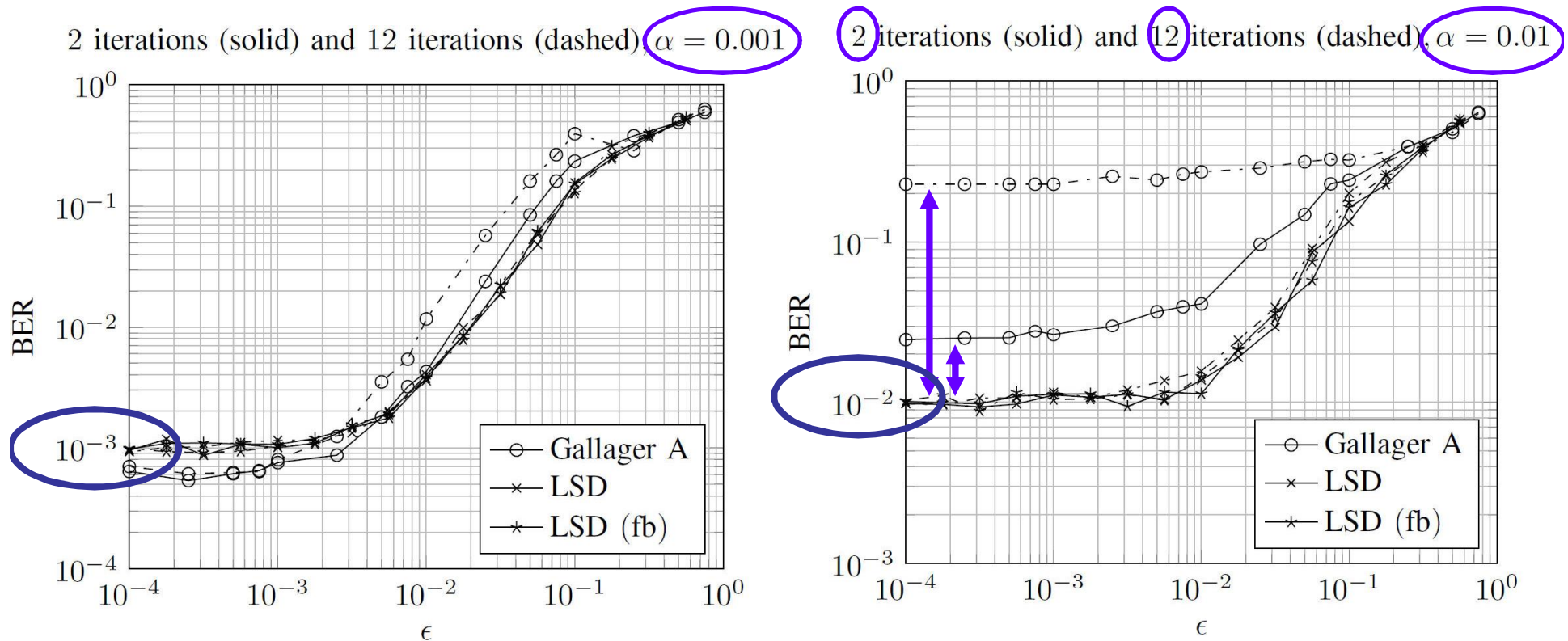


Fig. 9 Message-Passing Decoder with Space-Time Redundancy Technique. For instance, the Majority unit can be a 3-of-5 voter.

BER Results Without Space-Time Redundancy

WITHOUT Space-Time Redundancy

Internal Fault Injection: α
 $\mathbb{E}(3,6)$ LDPC code of length 64 over a BSC parameter of ϵ



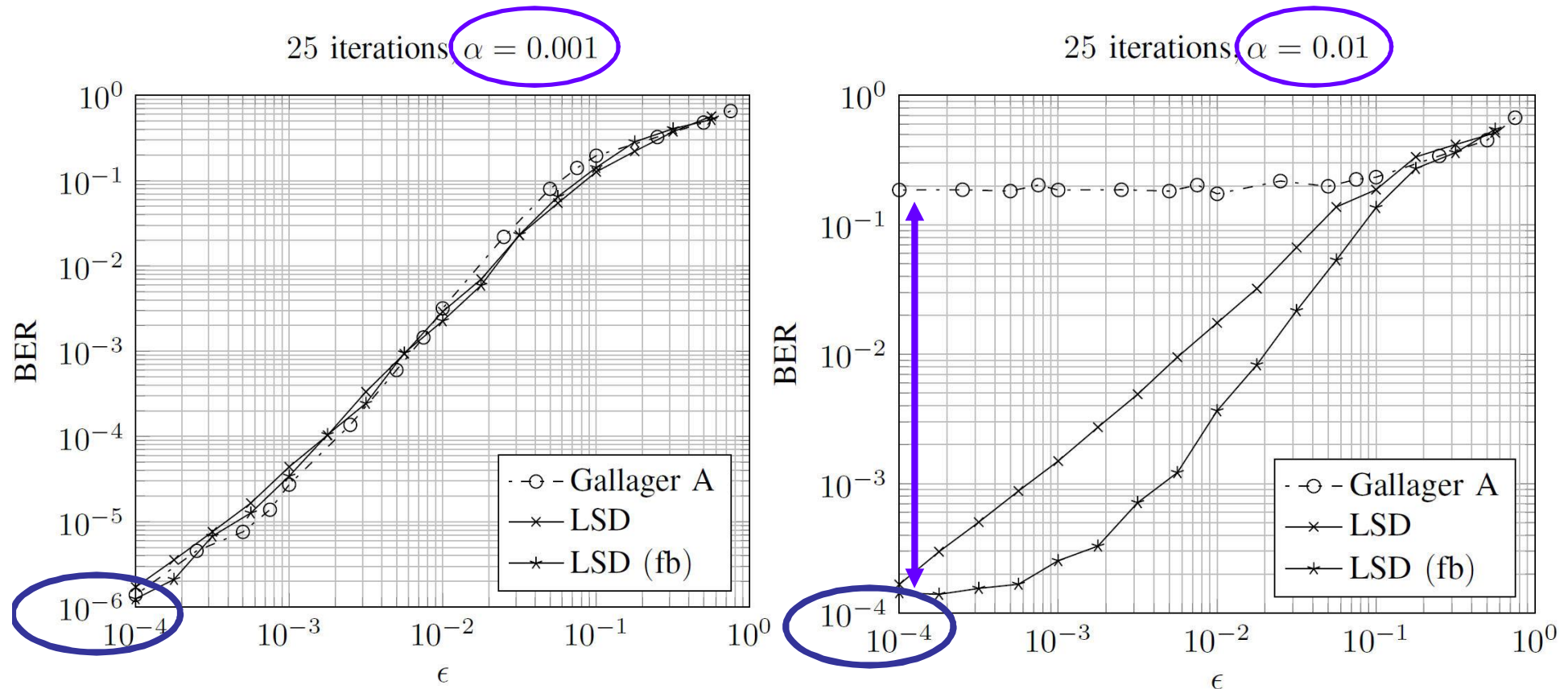
“ Gallager-A performance worsens with increased iterations when internal faults rate is high.

“ But LSD does not exhibit this degradation.

BER Results WITH Space-time Redundancy

WITH Space-Time Redundancy

Internal Fault Injection: α
 $\hat{E}(3,6)$ LDPC code of length 64 over a BSC parameter of ϵ



"The majority voter significantly improves the decoder's BER performance.

"Feedback-Mechanism is helpful as well.

OUTLINE

1. Emerging Challenge in Electronic Device

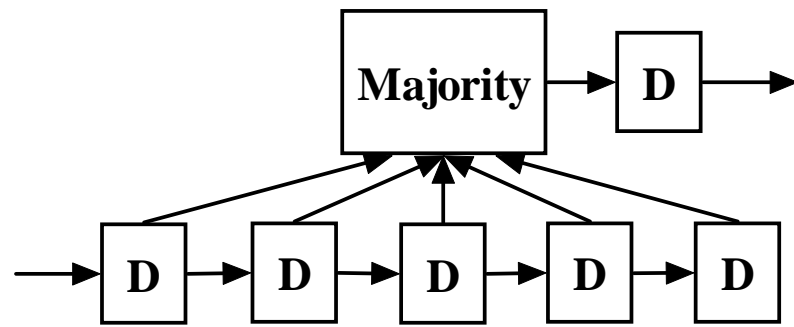
2. Previous Work: Coded Dual-Modular Redundancy (cDMR)

3. Latest Solution: A Decoder Against Internal Faults

4. Space-Time Redundancy Technique

5. Conclusions & Discussions

Discussions: Space-Time Redundancy Implementation



Easy Implementation for
Space-Time Redundancy Unit

Micro-Scale Circuit

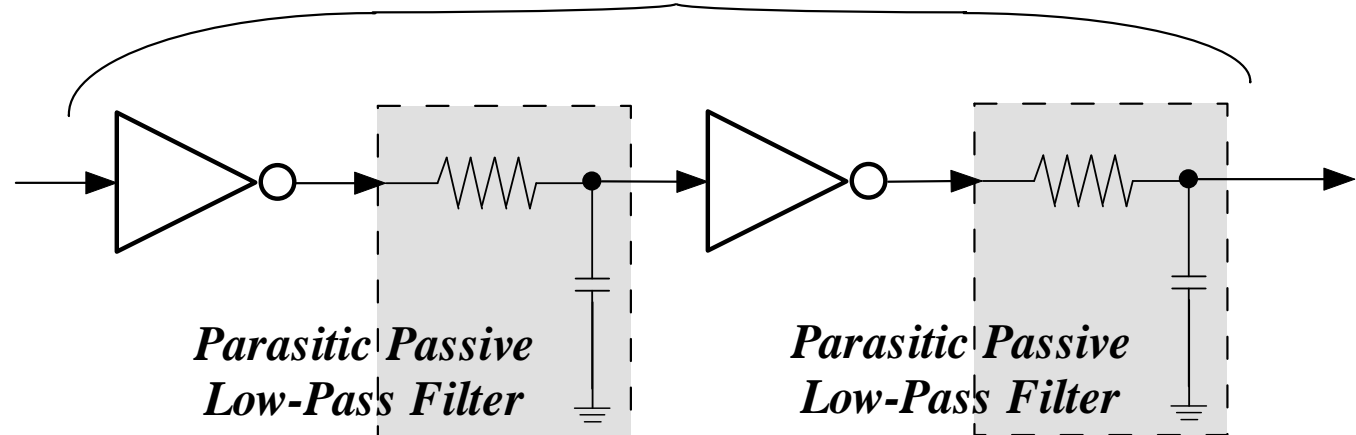


Fig. 10 This approach may be implemented, for instance, with the native R-C parasitics in a large-size output buffer.

Conclusions

“ Previous Work: A Decoder Against Internal Faults - LSD

- “ Gallager-A performance worsens with increased iterations when internal faults rate is high.
- “ But LSD does not exhibit this degradation.

“ Contributions: Feedback Mechanism

- “ Improve the error-resilience for embedded error-correction.

“ Contributions: Space-Time Redundancy Technique

- “ Requiring few overhead & Easy to be implemented as reliable unit.
- “ Significantly suppress internal faults.

“ Prospect: A Decoder Against Internal Faults

- “ A New Interesting Area: Embedded Error-Correction in Faulty Process.
- “ Still requiring further work to make it ripe for the application/implementation.

Acknowledgement



“This work was supported by the US National Science Foundation under award ECCS-0954747.



Thank You For Your Attention!

Back-ups: Threshold Determinations

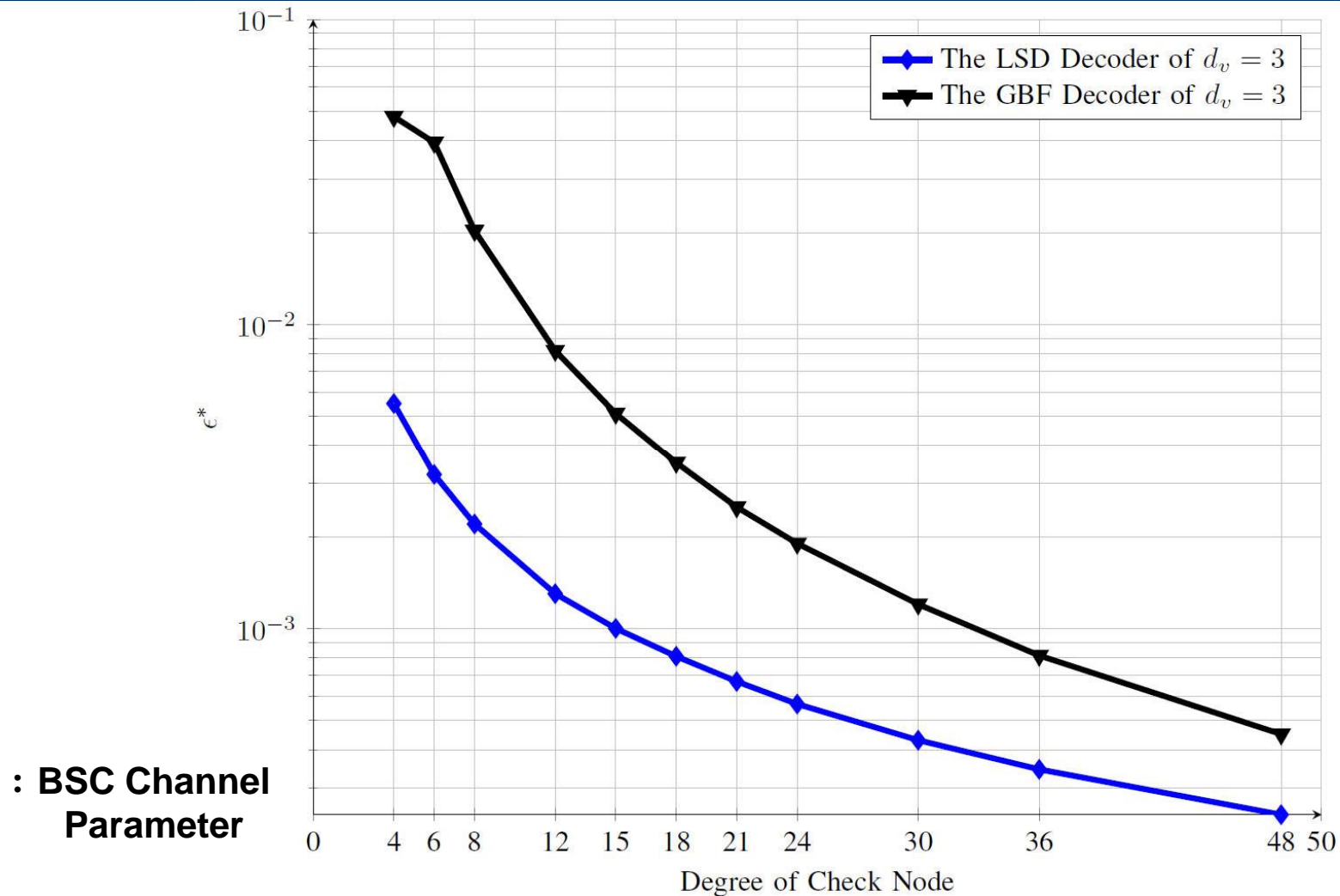
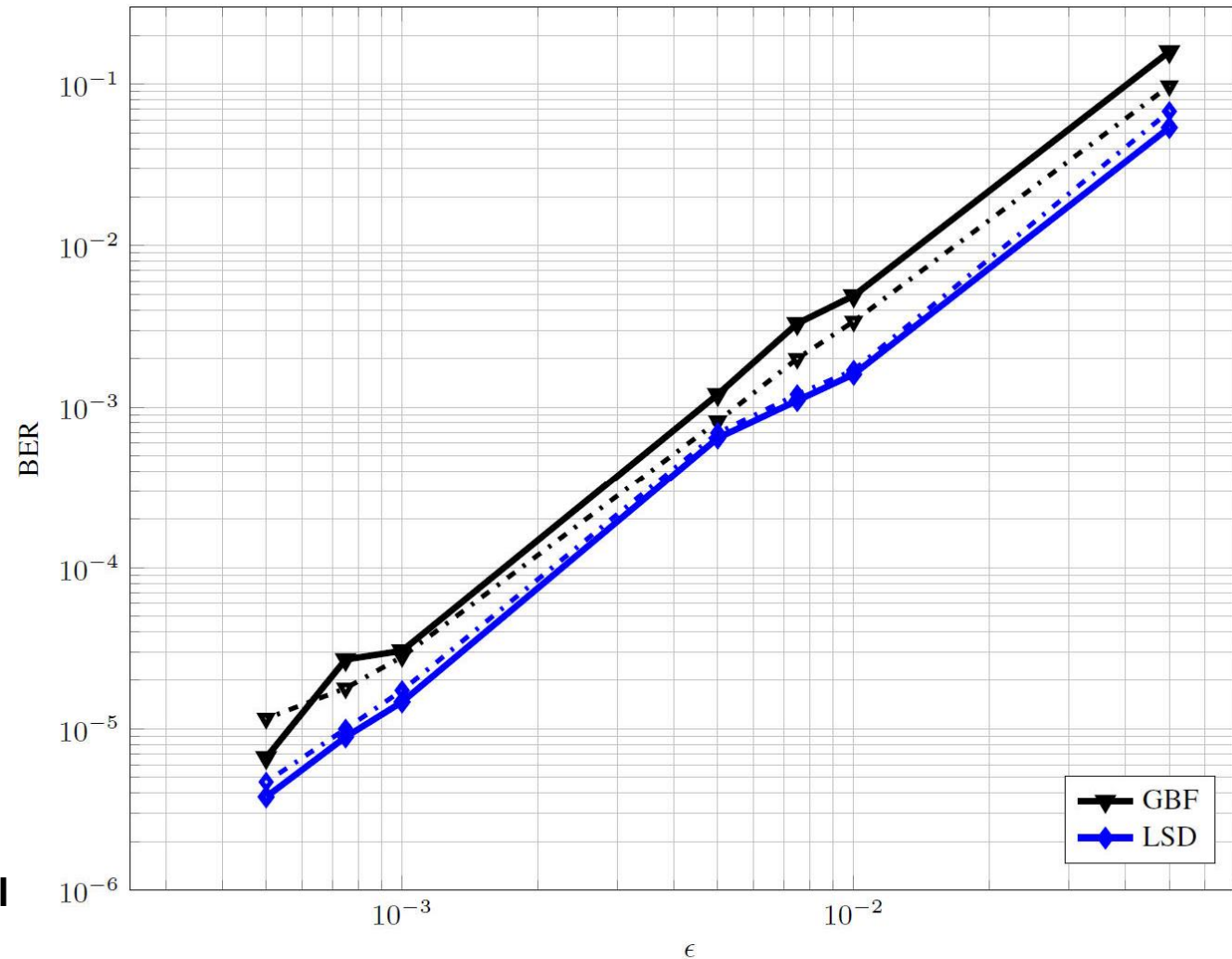


Fig. 11 Threshold of channel parameter over BSC for GBF (Gallager's Bit-Flipping method) and LSD, if the decoder process is error-free.

Back-ups: Special Case – Short-length Decoder



: BSC Channel
Parameter

Fig. 12 Simulation results of (3,6) LDPC code of length 64 under an error-free decoding process, dash lines for 2-iteration, solid lines for 20-iteration.

Back-ups: Threshold Determinations

	GBF	LSD			
	(d_v, d_c)	(d_v, d_c)	(d_v, d_c)	(d_v, d_c)	(d_v, d_c)
	(3,6)	(3,6)	(3,12)	(3,24)	(3,48)
α^*	0.0082	0.0303	0.0096	0.0032	0.0011
ϵ^*	0.0126	0.0690	0.0199	0.0059	0.0011

- : Decoder ~~B~~ Internal Transient Error Rate
- : BSC Channel Parameter

Tab. 3 Maximal Parameter α^* and Maximal Parameter ϵ^* are determined when it is beneficial to use the decoder under a faulty decoder process.