Serial and Parallel Processing Architecture for Signal Synchronization

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Outline

I. Introduction

This document presents parameters of the design of a serial and a parallel architecture for time synchronization of the BPSK, QPSK, 8PSK, 16APSK, 32APSK and 64APSK signals of the DVB-S2 standard. The architecture is able to work at low ratio Es/No (Ratio between the energy per transmitted symbol and single sided noise power**)**. The Gardner algorithm is used to calculate the timing error. The timing recovery is performed using a Nyquist filter (Square-Root Raised Cosine filter) and an interpolation filter, these two filters are combined in a single filter to reduce the number of multiplications and additions.

The serial architecture processes one symbol per clock cycle, whereas that the parallel architecture processes four symbols per clock cycle; each symbol is represented only by two samples.

The communication system is assume to have stable emission clock and a receiver clock with a precision of 5 ppm (standard deviation of the variation of the number of clock cycles per million) and 50 ppm, with the clock frequency of the receiver slightly higher than the clock frequency of the transceiver. Assuming that T is the emission period of one symbol in the transceiver, then in the receiver the symbol period is $(1-\varepsilon)T$ where $\varepsilon = PPM/(10^6 + PPM)$ and PPM =5ppm, 10ppm, etc. The value of ε can be taken as 5×10^{-5} in order to work with PPM =50ppm. Note that there are two samples per period to respect the Nyquist sampling rate.

The BER curve is presented to show the performance of these architectures with fixed point simulation in MATLAB. The VHDL code of these architectures is simulated with ModelSim with the same input source as in MATLAB.

For serial and parallel architecture, the input samples are represented by seven bits, while the output symbols are represented by eight bits. Both architectures have input signals called ***clk***, ***rst*** and ***go***, ***clk*** is clock signal, ***rst*** is a signal that puts these architectures in initial conditions and ***go*** is a signal which allows operation of both architectures. Both architectures have an output signal called ***write_data***, this signal allows write a memory or register in correct time because these architectures can operate with different values of ppm. Fig. 1 shows all input and output signals.

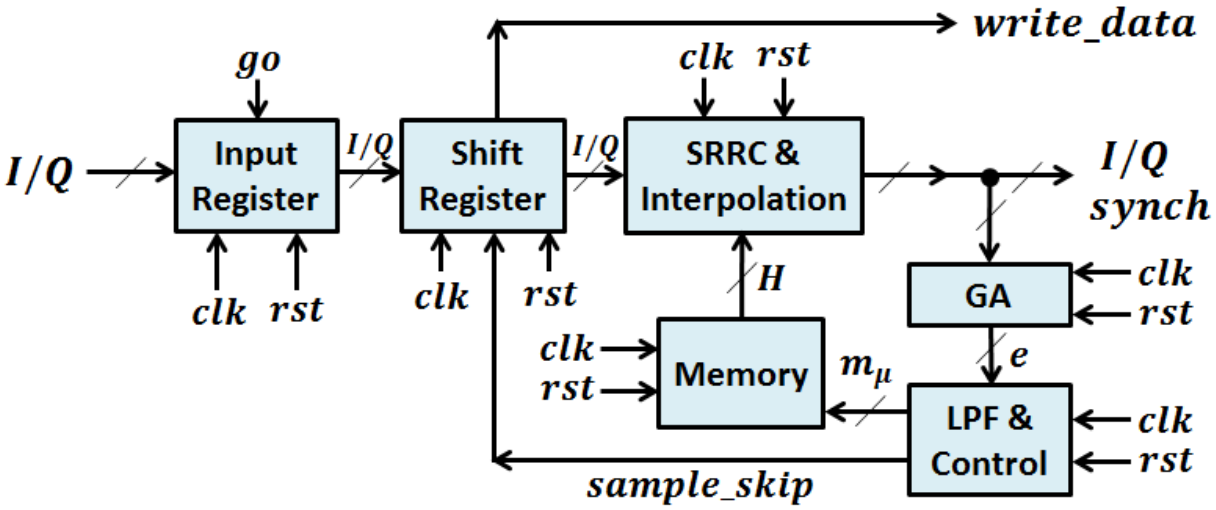

Fig. 1: serial and parallel architecture.

The Input Register component: is a simple register that has an input of 8 samples in the parallel architecture, whereas that in the serial architecture has an input of 2 samples.

Thanks to a Shift Register component and an appropriate control, the hardware implementation skips 8 samples in one clock cycle to guarantee the parallel process of 8 samples per clock cycle in the parallel architecture. Whereas that in serial architecture; this component skips 2 samples in one clock cycle.

The SRRC & Interpolation component performs the filtering process between the filter coefficients stored in the Memory component (***H*** signal) and samples coming from the Shift Register component, this filtering is done in parallel in order to process 8 samples per clock cycle in parallel architecture. Outputs of this component are symbol synchronized which help to estimate the timing error for the next samples which will be filtered.

The Gardner Algorithm (GA) component does the timing error estimation using the Gardner algorithm [1]. The output of this component is a signal called ***e***.

The Low pass filter and Control (LPF & Control) component does the filtering of timing errors (***e*** signal) using a simple low pass filter, this component generates control signals called ***sample_skip*** and $\boldsymbol{m_\mu}$. The ***sample_skip*** signal helps to skip a sample in the Shift Register component, whereas that $\boldsymbol{m_\mu}$ signal helps to choose coefficients of the SRRC & Interpolation filter, i.e. $\boldsymbol{m_\mu}$ signal indicates a memory address.

The Memory component stores the filter coefficients precomputed previously, this component is a finite memory.

II. Results in MATLAB

Simulations with different values of roll-off factor are presented below, here is only considered the parallel architecture because the serial and parallel architecture have the same performance. Theoretical BER for the 16APSK, 32APSK and 64APSK modulations were obtained with Monte Carlo method.

QPSK, 8PSK and 16APSK symbols shall be generated according to DVB-S2 standard [2].

BPSK, 32APSK (4+12+16rbAPSK, code rate 2/3, normal FECFRAME) and 64APSK (4+12+20+28APSK, code rate 132/180) symbols shall be generated according to DVB-S2X standard [3].

II.1 Simulation result with roll-off equal to 0.35

Fig. 2 compares the BER simulation results of the theoretical BER and BER of the parallel architecture with a Variation of the Number of Clock Cycle (VNCC) of 5 ppm between the transmitter and the receiver.

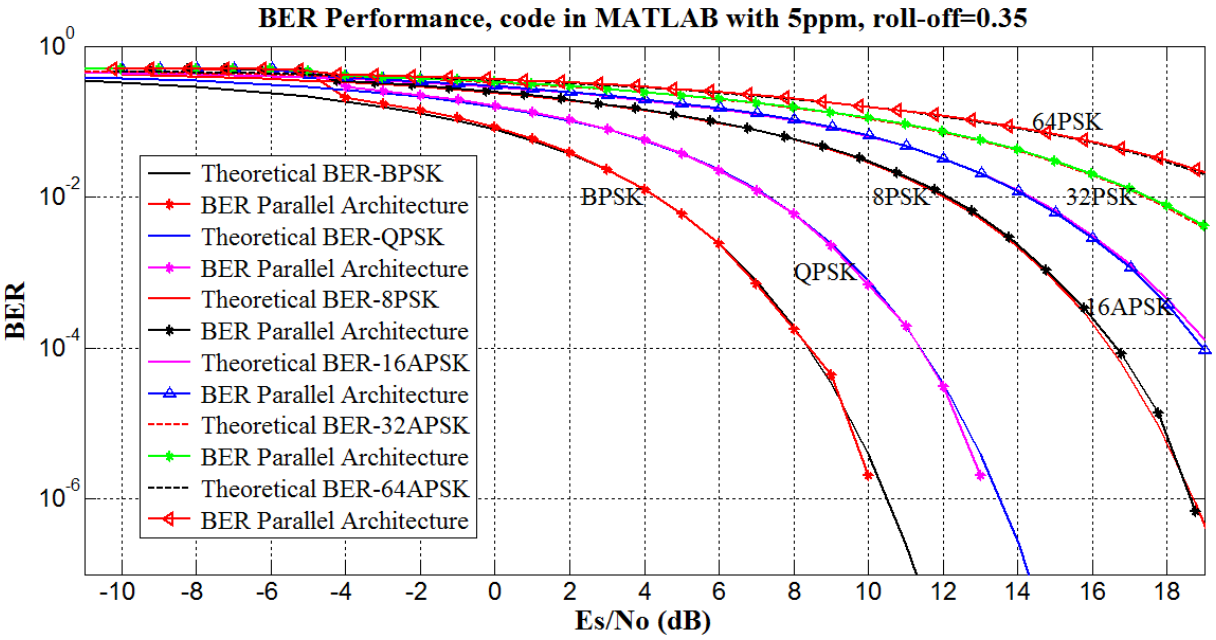

Fig. 2 BER simulation results with VNCC = 5 ppm.

When Es/No is less than -4dB, both serial and parallel architecture cannot recover the signal as show the Fig. 3, this figure is the result to make a zoom between -12 dB and 6 dB in the Fig. 2.

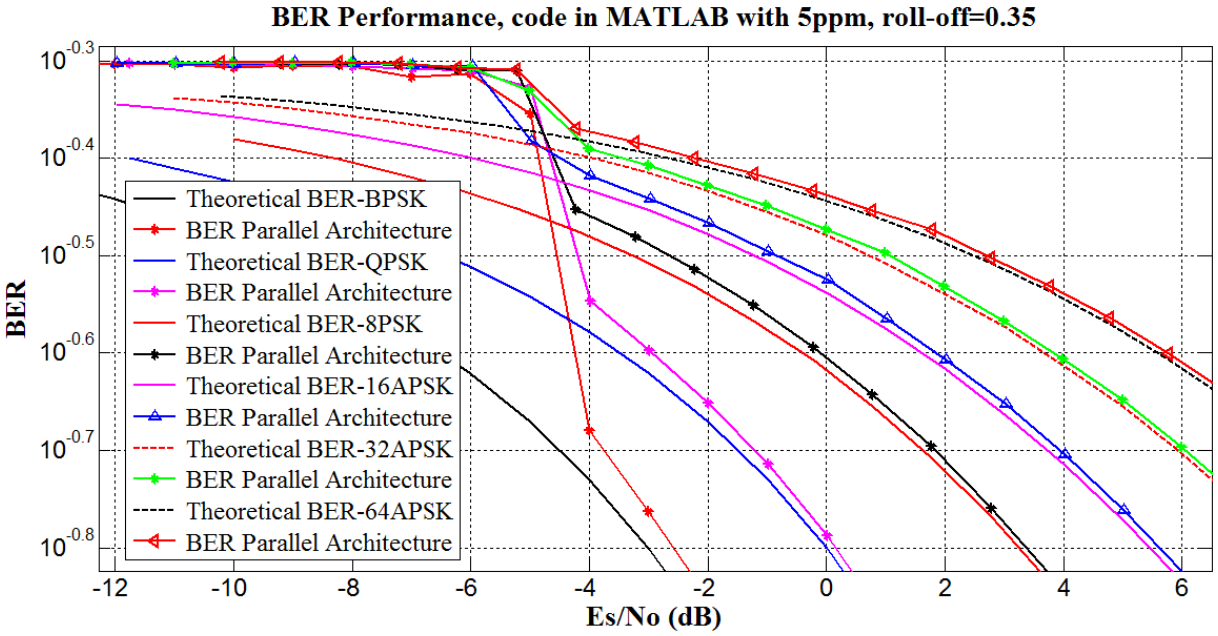

Fig. 3: BER simulation results with VNCC = 5 ppm. For Es/No between -12 dB and 6 dB. Note that timing synchronization fails when Es/No < -4dB

Fig. 4 compares the BER simulation results of the theoretical BER and BER of the parallel architecture with VNCC = 50 ppm between the transmitter and the receiver.

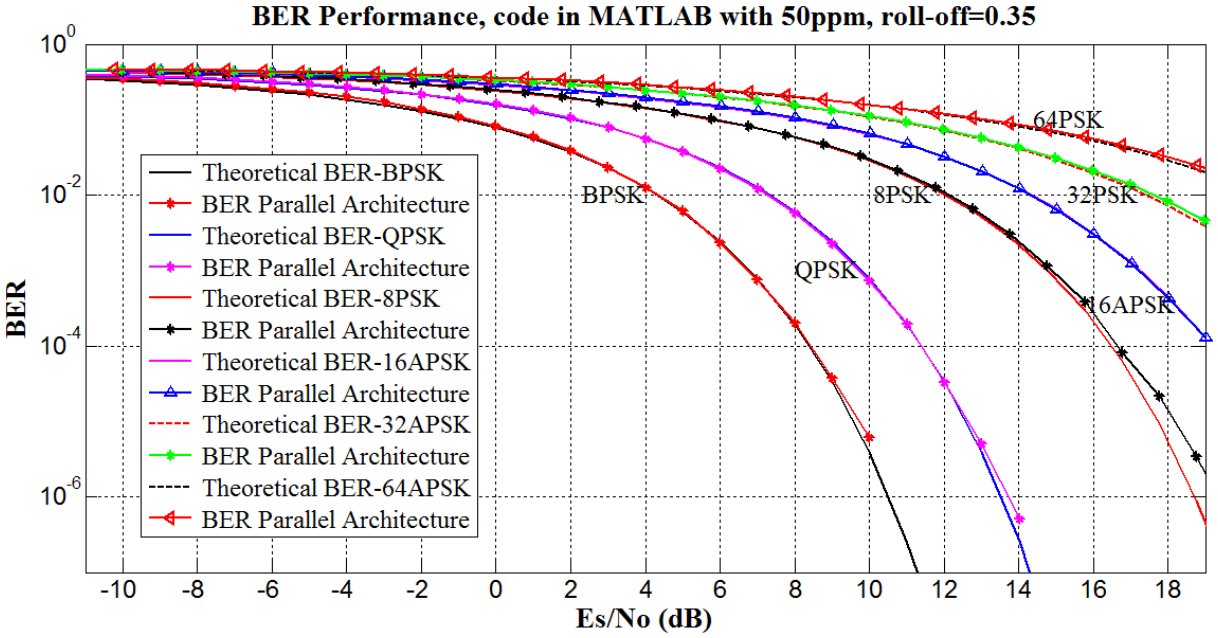

Fig. 4: BER simulation results with VNCC = 50 ppm.

Fig.5 is the result of making a zoom between -12 dB and 6 dB in the Fig. 4. This figure shows that the serial and parallel architecture can recover the good timing synchronization up to -10 dB, i.e. within the DVB-S2X standard.

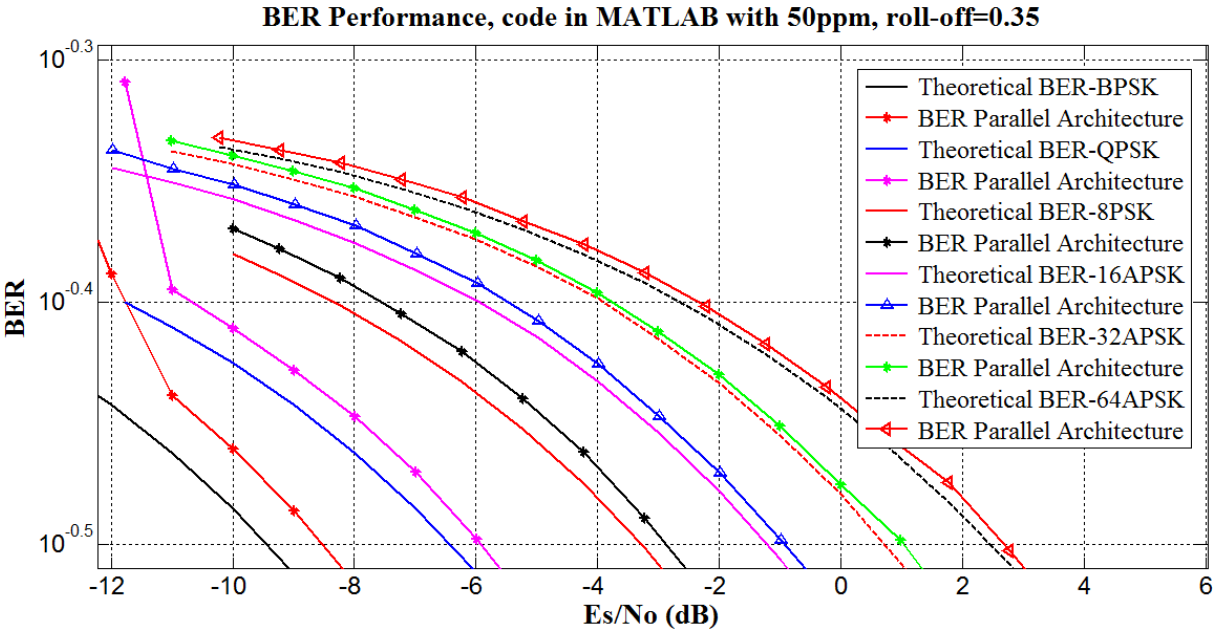

Fig. 5: BER simulation results with VNCC = 50 ppm. For Es/No between -12 dB and 6 dB. Note that timing synchronization fails when Es/No < -10dB

II.2. Simulation result with roll-off equal to 0.20

Fig. 6 compares the BER simulation results of the theoretical BER and BER of the parallel architecture with VNCC = 5 ppm between the transmitter and the receiver.

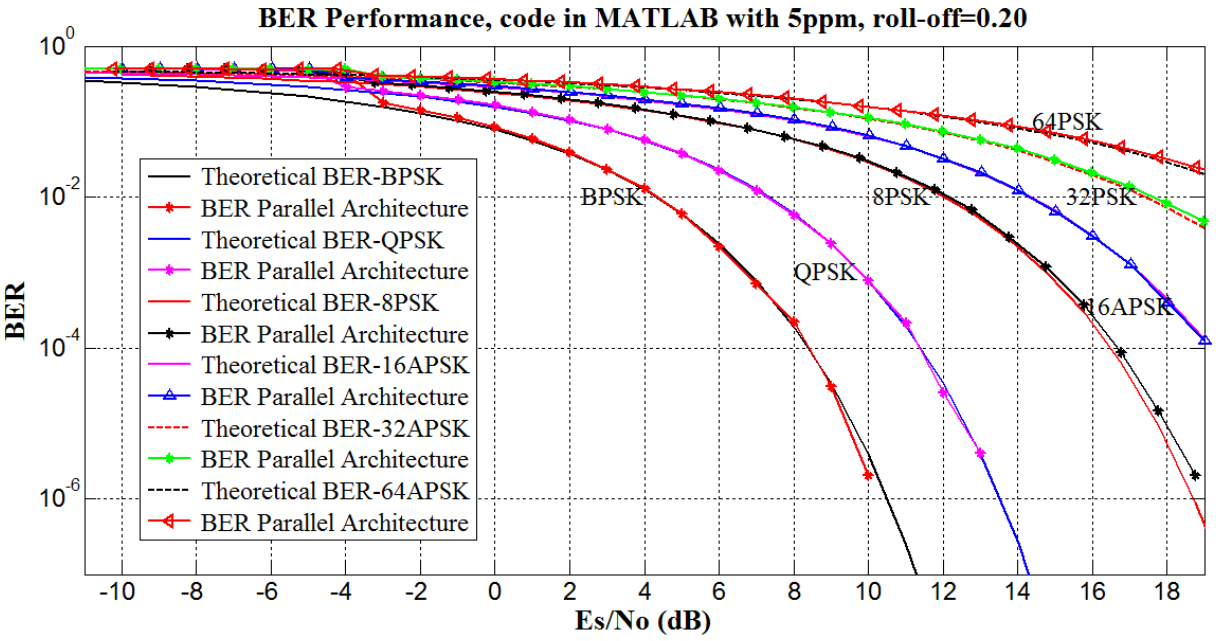

Fig. 6 BER simulation results with VNCC = 5 ppm.

When Es/No is less than -3dB, both serial and parallel architecture cannot recover the signal as show the Fig. 7, this figure is the result of making a zoom between -11 dB and 4 dB in the Fig. 6.

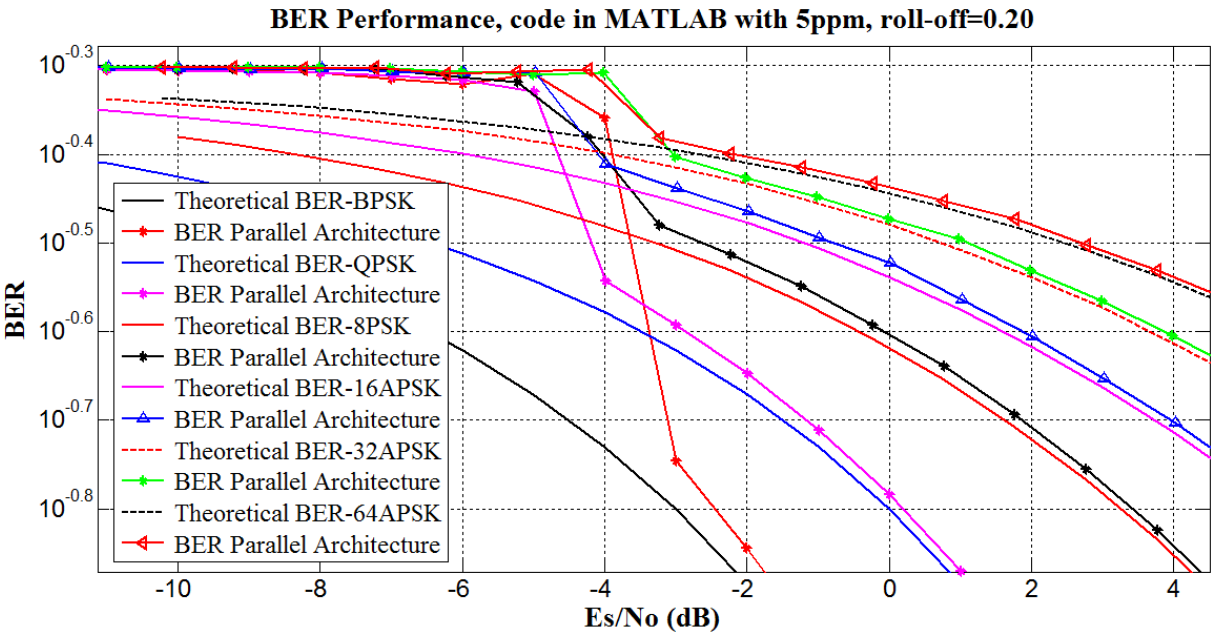

Fig. 7: BER simulation results with VNCC = 5 ppm. For Es/No between -10 dB and 4 dB. Note that timing synchronization fails when Es/No < -3dB

Fig. 8 compares the BER simulation results of the theoretical BER and BER of the parallel architecture with VNCC = 50 ppm between the transmitter and the receiver.

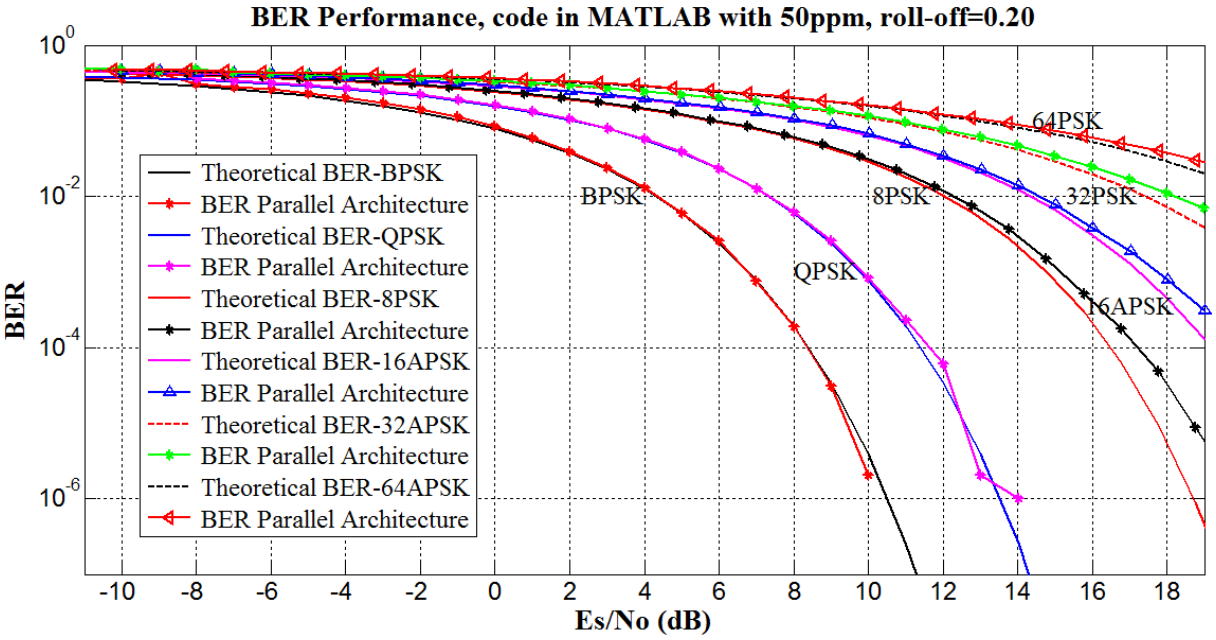

Fig. 8: BER simulation results with VNCC = 50 ppm.

Fig.9 is the result of making a zoom between -12 dB and 4 dB in the Fig. 8. This figure shows that the serial and parallel architecture can recover the right timing synchronization up to -7 dB.

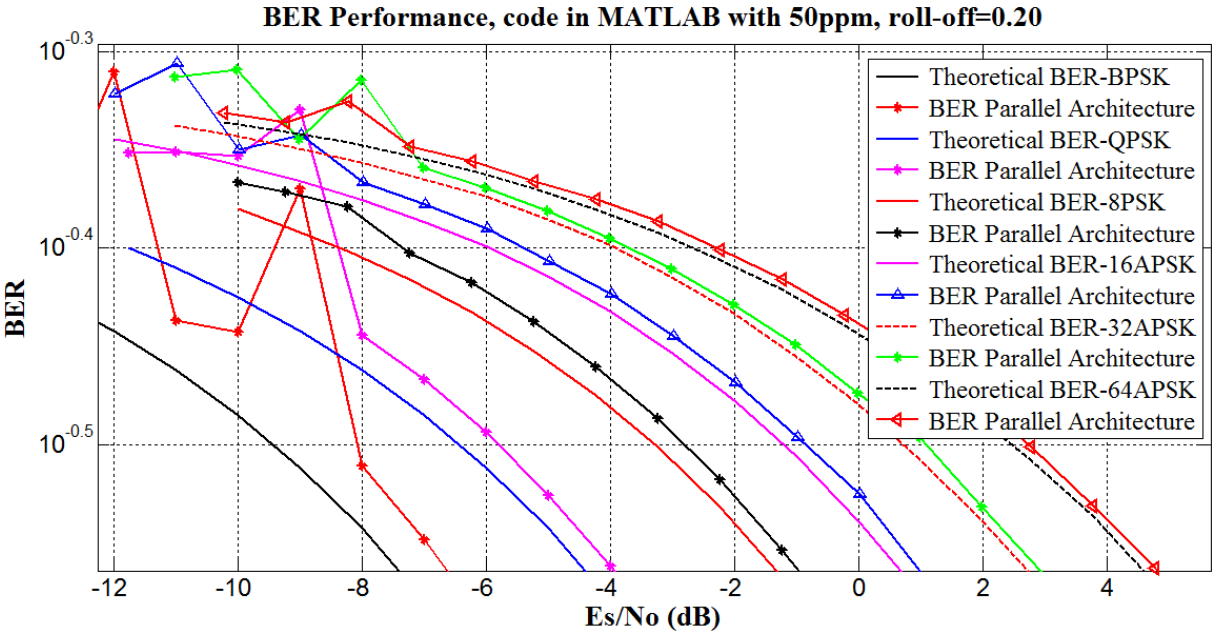

Fig. 9: BER simulation results with VNCC = 50 ppm. For Es/No between -12 dB and 4 dB. Note that timing synchronization fails when Es/No < -7dB

II.3. Simulation result with roll-off equal to 0.10

Simulations with the roll-off factor equal to 0.10 show that the performance of the parallel architecture is not good and much information is lost. Fig. 10 and Fig. 11 show the results.

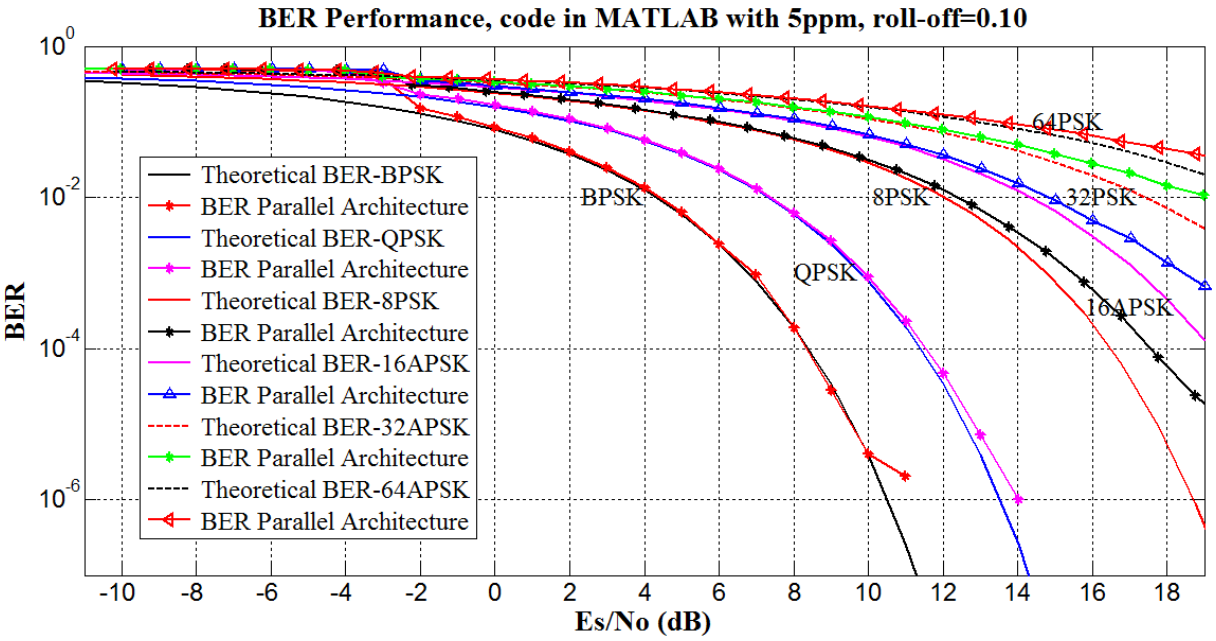

Fig. 10: BER simulation results with VNCC = 5 ppm.

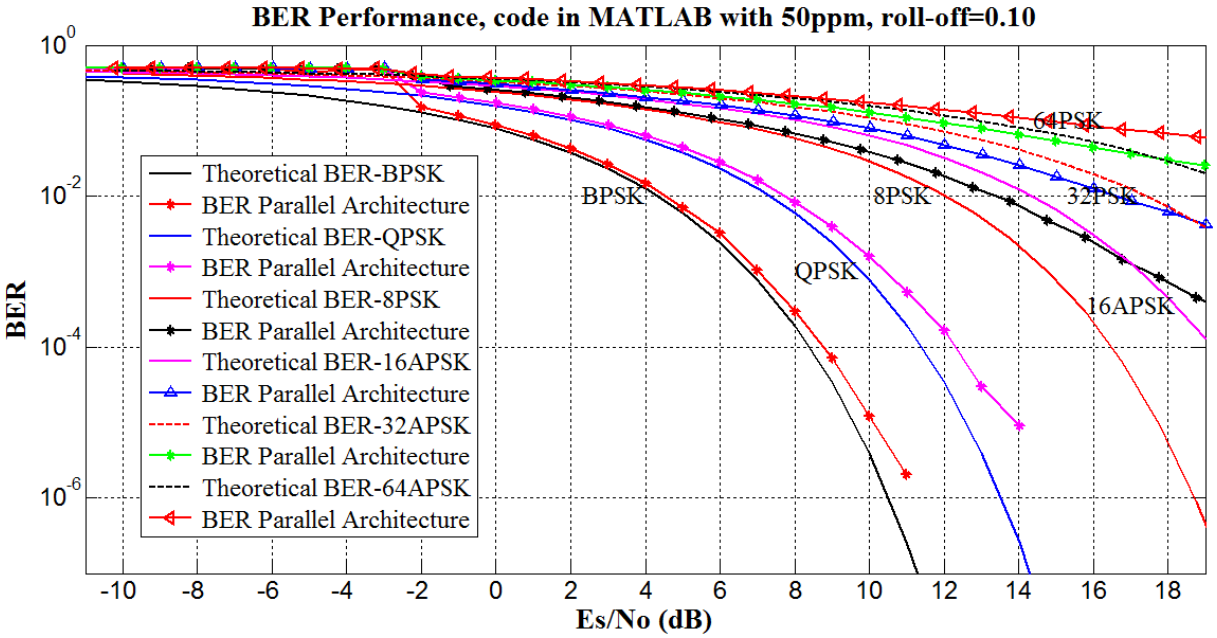

Fig. 11: BER simulation results with VNCC = 50 ppm.

II.4. Simulation result with roll-off equal to 0.10

Simulations with the roll-off factor equal to 0.05 show that the performance of the parallel architecture is bad and too much information is lost. Fig. 12 and Fig. 13 show these results.

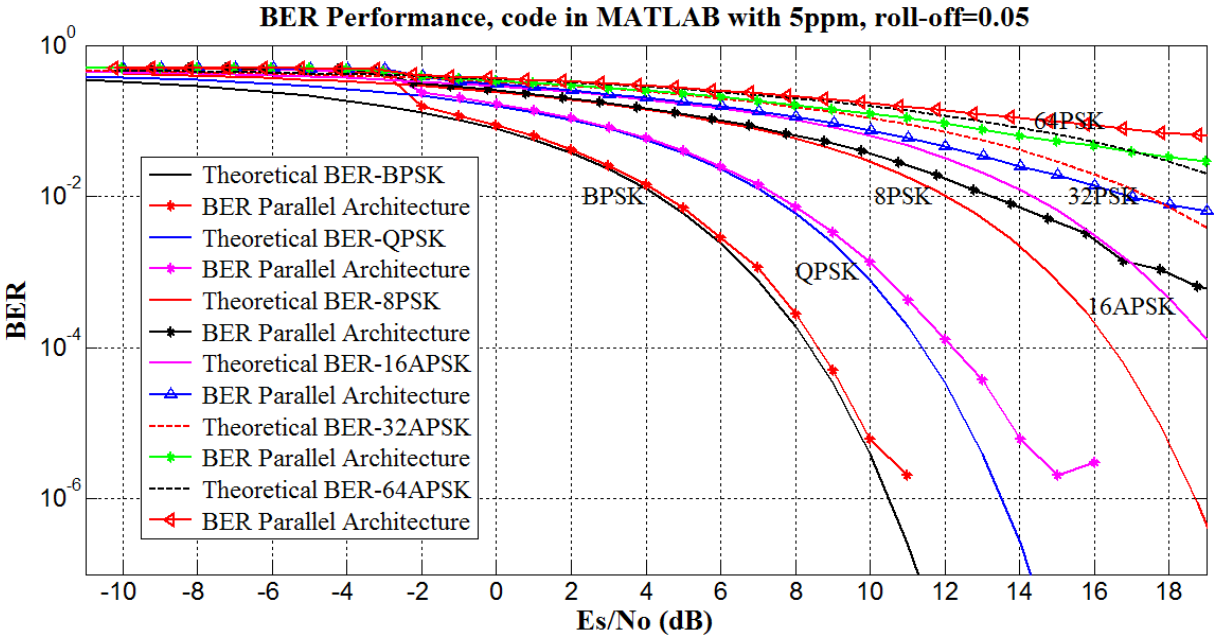

Fig. 12: BER simulation results with VNCC = 5 ppm.

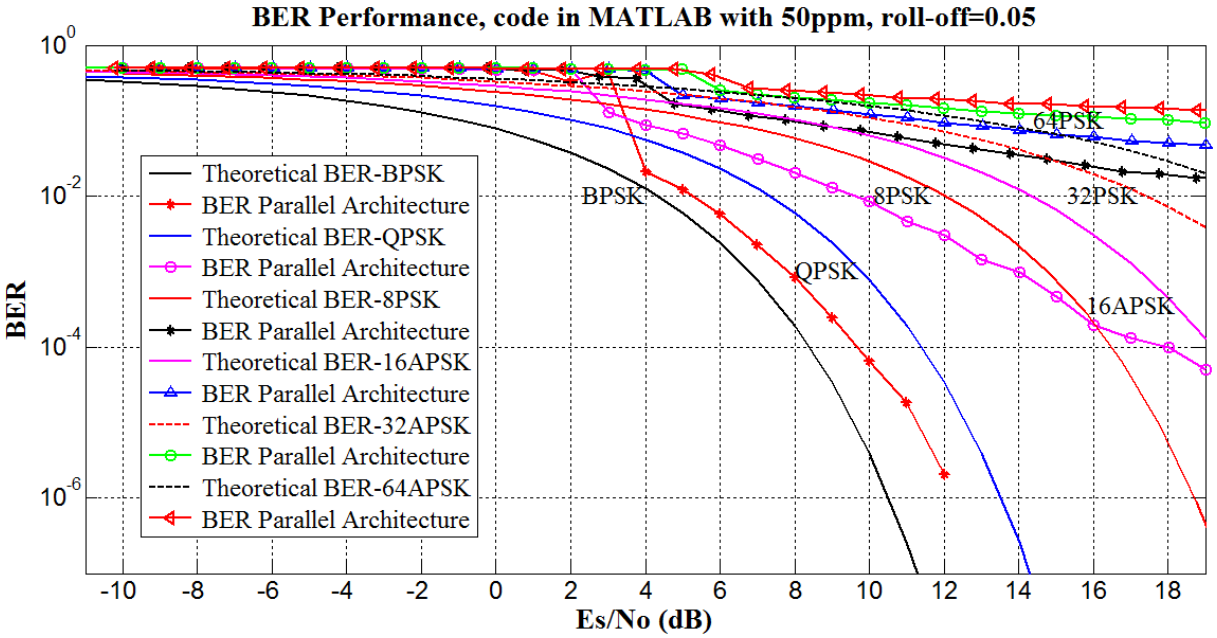

Fig. 13: BER simulation results with VNCC = 50 ppm.

III. Results in MATLAB and VHDL code

III.1. QPSK modulation

Fig. 14 compares the BER simulation results of the theoretical BER, BER of the serial architecture in MATLAB and BER of the serial architecture in VHDL code, a VNCC of 50 ppm between the transmitter and receiver is simulated.

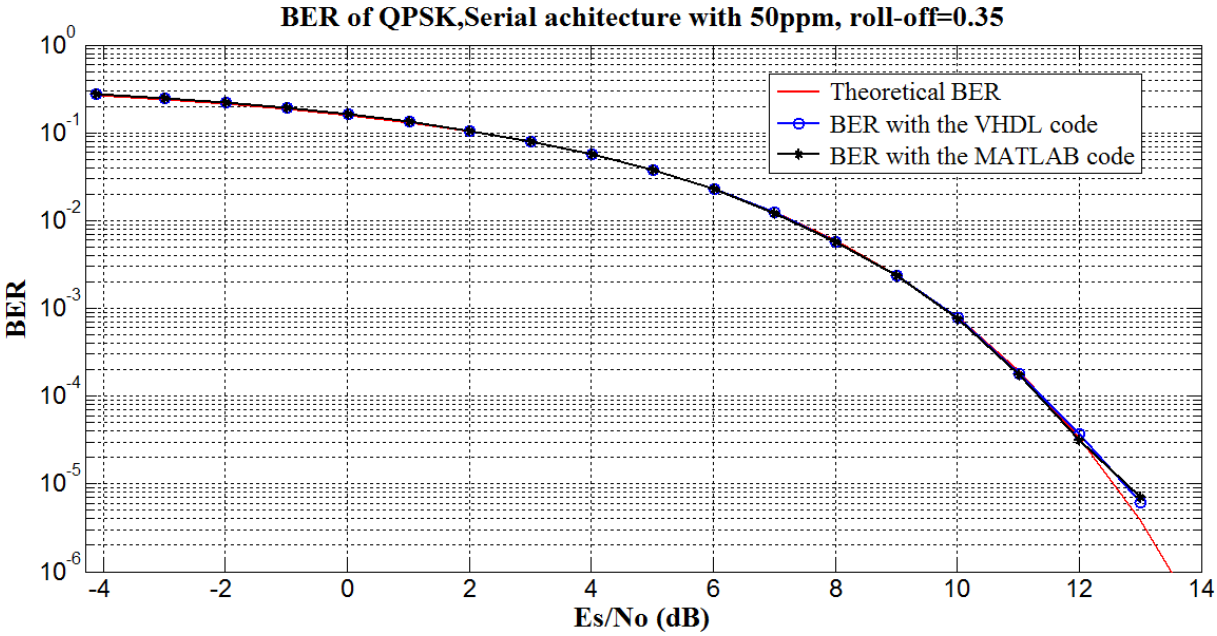

Fig. 14: BER simulation results for serial architecture.

Fig. 15 compares the BER simulation results of the theoretical BER, BER of the parallel architecture in MATLAB and BER of the parallel architecture in VHDL code, a VNCC of 50 ppm between the transmitter and receiver is simulated.

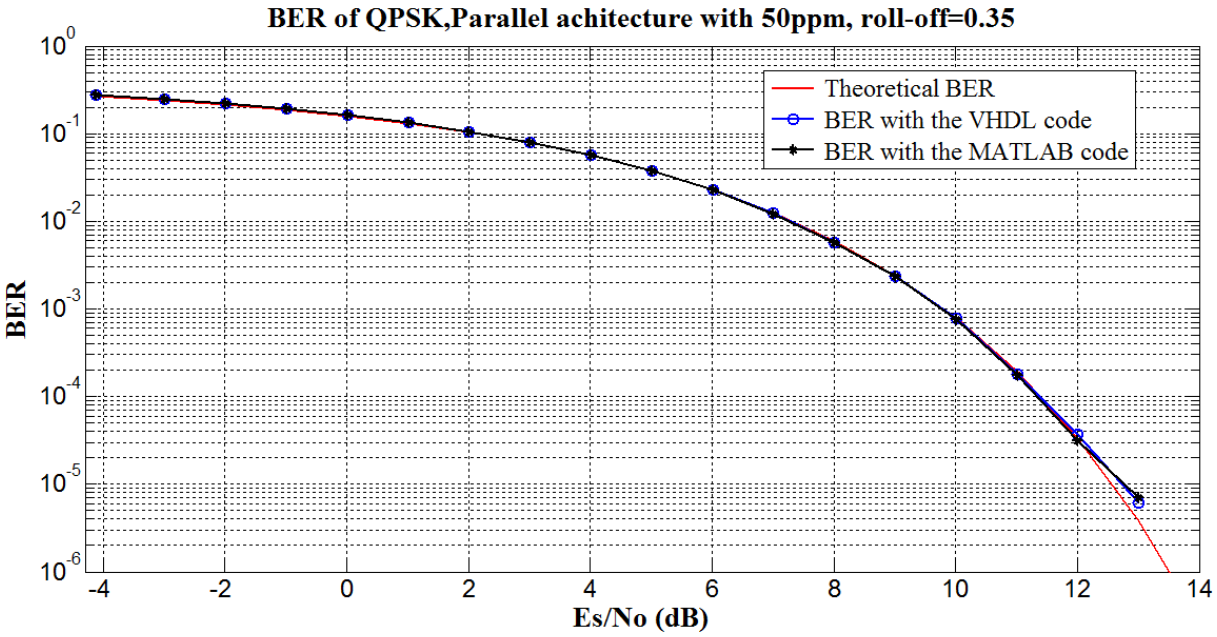

Fig. 15: BER simulation results for parallel architecture.

III.2. 8-PSK modulation

Fig. 16 compares the BER simulation results of the theoretical BER, BER of the serial architecture in MATLAB and BER of the serial architecture in VHDL code, a VNCC of 50 ppm between the transmitter and receiver is simulated.

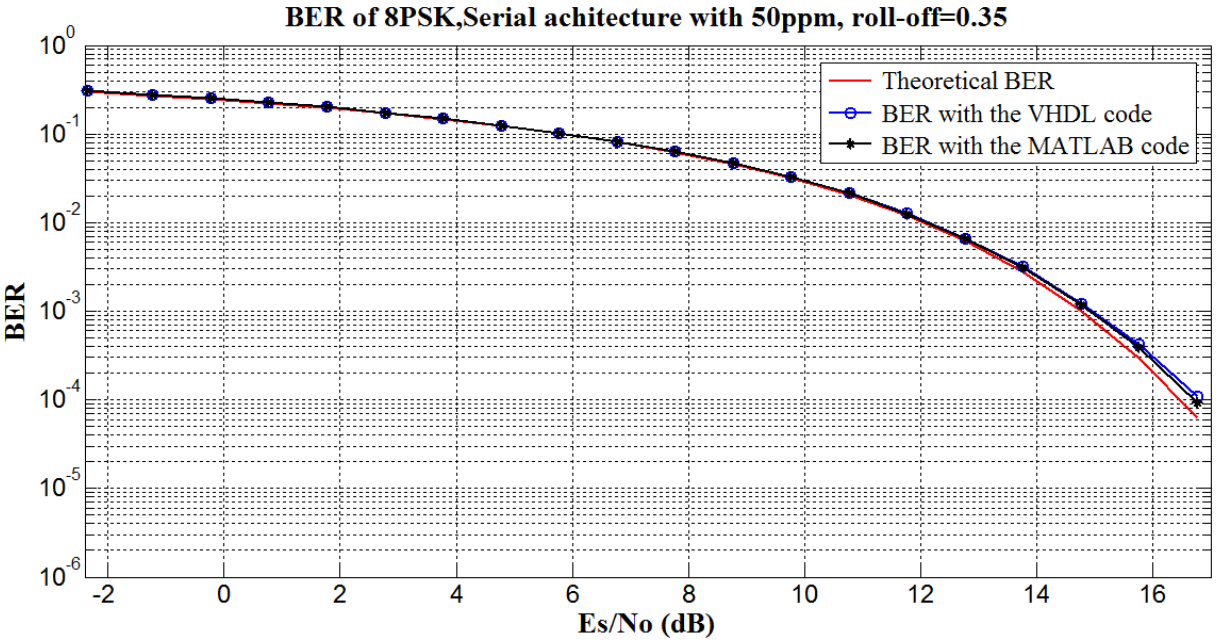

Fig. 16: BER simulation results for serial architecture.

Fig. 17 compares the BER simulation results of the theoretical BER, BER of the parallel architecture in MATLAB and BER of the parallel architecture in VHDL code, a VNCC of 50 ppm between the transmitter and receiver is simulated.

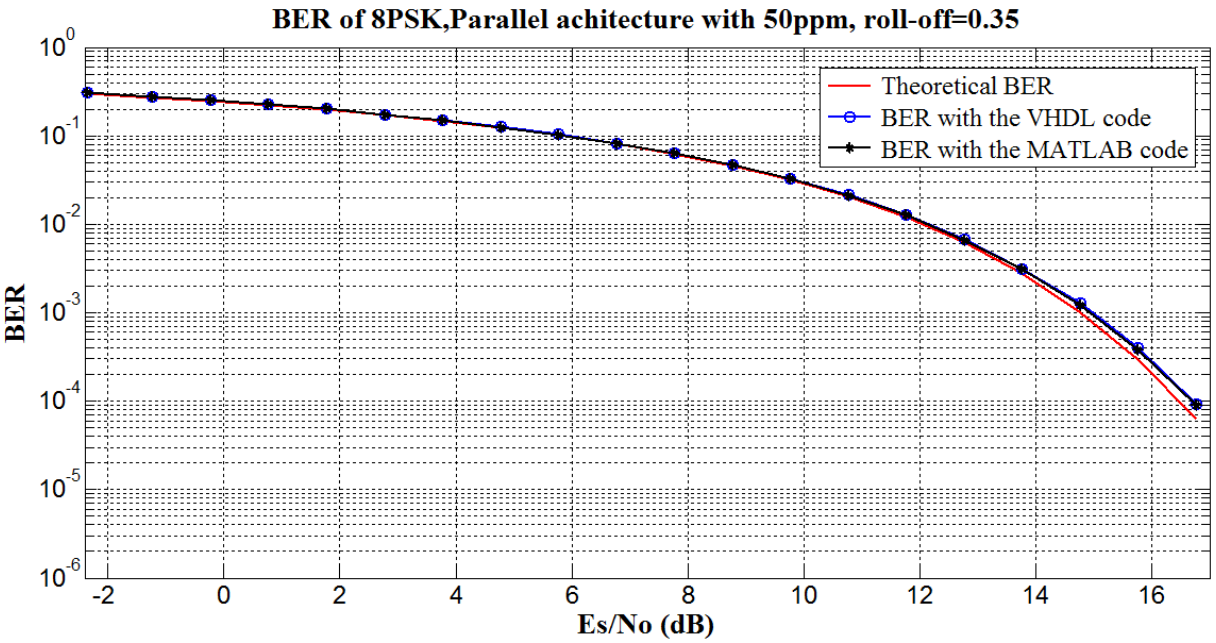

Fig. 17: BER simulation results for parallel architecture.

IV. Device Utilization Summary

In this section, we present the synthesis result on two FPGA families (Virtex and Altera) as well as on the ST Microelectronics 65 nm technology.

IV.1. Synthesis results on Xilinx FPGA

When the VHDL has been synthetized on a Xilinx XC6VLX240T-3FF1156 FPGA chip, the obtained maximum frequency is 281 MHz, on both parallel and serial architecture. The raw input bit throughput both architectures is thus given table 1:

Constellation	Serial architecture	Parallel architecture
BPSK	0.281 Gbit/s	1.124 Gbit/s
QPSK	0.562 Gbit/s	2.248 Gbit/s
8-PSK	0.843 Gbit/s	3.372 Gbit/s
16-APSK	1.124 Gbit/s	4.496 Gbit/s
32-APSK	1.405 Gbit/s	5.620 Gbit/s
64-APSK	1.686 Gbit/s	6.744 Gbit/s

Table 1: Achievable raw input bit throughput for the architecture

a) Serial architecture

Logic utilization	Used	Available	Utilization
Number of Slice Registers	2964	301440	0%
Number of Slice LUTs	5572	150720	3%
Number of fully used LUT-FF pairs	2347	6189	37%
Number of BUFG/BUFGCTRLs	1	32	3%

b) Parallel architecture

Logic utilization	Used	Available	Utilization
Number of Slice Registers	8682	301440	2%
Number of Slice LUTs	21202	150720	14%
Number of fully used LUT-FF pairs	7651	22233	34%
Number of BUFG/BUFGCTRLs	2	32	6%

IV.2. Synthesis results on Altera FPGA

When the VHDL has been synthetized on an Altera EP3SL150F1152C2 FPGA chip, the obtained maximum frequency is 276 MHz on serial architecture and 248 MHz on parallel architecture.

a) Serial architecture

Logic utilization	Used	Available	Utilization
Combinational ALUTs	969	113600	0.85%
Dedicated logic registers	1679	113600	1%
DSP block 18-bit elements	74	384	19%

b) Parallel architecture

Logic utilization	Used	Available	Utilization
Combinational ALUTs	2635	113600	2%
Dedicated logic registers	3635	113600	3%
DSP block 18-bit elements	296	384	77%

V. Intrinsic noise

In this section, we derive the Mean Square Error (MSE) due to: 1) the quantization of the input symbol (Intrinsic Noise of the Quantization of Input Data, or INQID), 2) the INQID and the imperfection of the half Nyquist filter, the interpolation filter and the residual timing error (Intrinsic Noise of the Parallel Architecture or INPA). Both INQID and INPA are given as a function of $\boldsymbol{n}$, the number of bits used to sample the input analog signal.

V.1. Intrinsic Noise of the Quantization of Input Data (INQID)

Fig. 18 shows the diagram to calculate the error committed when the signal is quantified

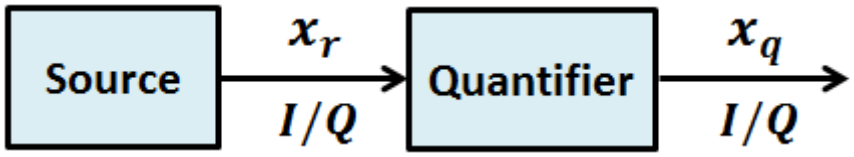

Fig. 18: Diagram to calculate the INQID.

To demonstrate the effects of quantization on the signal $\boldsymbol{x_r}$, it uses the next equation.

$$\tilde{\boldsymbol{x}} = \left\lfloor \frac{\boldsymbol{x_r} \times \boldsymbol{2^n}}{\boldsymbol{x_{rmax}}} + \boldsymbol{0.5} \right\rfloor \times \frac{\boldsymbol{x_{rmax}}}{\boldsymbol{2^n}}$$

Where $\lfloor x \rfloor$ represents the highest integer that is smaller of equal to x, n is the number of bits of samples and $\boldsymbol{x_{rmax}}$ is the largest element of $\boldsymbol{x_r}$.

INQID can be written as:

$$\mathbf{INQID} = \frac{\boldsymbol{1}}{\boldsymbol{k}} \left(\sum_{\boldsymbol{i=1}}^{\boldsymbol{k}} |\tilde{\boldsymbol{x}} - \boldsymbol{x_r}|^2 \right)$$

Where $|x|$ represents the complex magnitude of x, k the index of constellation point and $\boldsymbol{x_r}$ the constellation point defined in the DVB-S2X standard.

V.2. Intrinsic Noise of the Parallel Architecture (INPA)

Fig. 19 shows the diagram to calculate the error committed when the signal is quantified and processed for the parallel architecture.

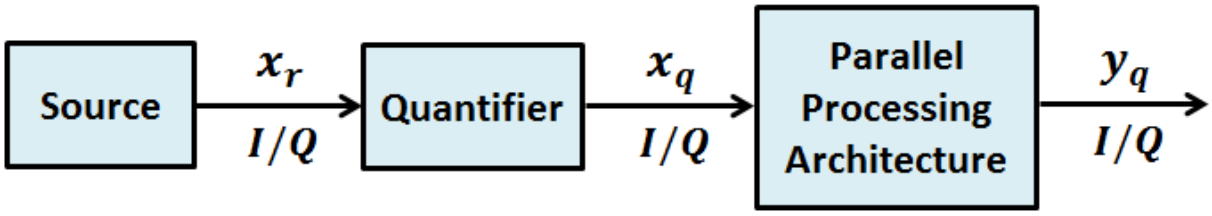

Fig. 19: Diagram to calculate the INPA.

The quantized value $\boldsymbol{x_q}$ of $\boldsymbol{x_r}$ on n bits is given by:

$$\boldsymbol{x_q = \left\lfloor \frac{x_r \times 2^n}{x_{rmax}} + 0.5 \right\rfloor}$$

Where $\lfloor x \rfloor$ represents the highest integer that is smaller of equal to x, n is the number of bits of samples and $\boldsymbol{x_{rmax}}$ is the largest element of x.

The equation used to computation of different values of $\boldsymbol{y_q}$ is:

$$\boldsymbol{y_q(k) = \sum_{i=-\frac{w}{2}}^{+\frac{w}{2}} x_q(i) h_q(k-i)}$$

Where $\boldsymbol{h_q}$ is the impulse response of SRRC and Interpolation filter, w+1 is the length of the filter.

INPA can be written as:

$$\boldsymbol{\tilde{y} = \frac{y_q}{2^n}}$$

$$\boldsymbol{\text{INPA} = \frac{1}{k}\left(\sum_{i=1}^{k} |\tilde{y} - x_r|^2\right)}$$

Where $|x|$ represents the complex magnitude of x.

n	INQID	INPA
1	8.5584×10^{-2}	0.99999
2	4.2787×10^{-2}	1.5563×10^{-1}
3	1.836×10^{-3}	1.6748×10^{-2}
4	1.836×10^{-3}	5.0556×10^{-3}
5	3.8323×10^{-4}	1.4336×10^{-3}
6	1.3539×10^{-4}	5.5590×10^{-4}
7	1.5763×10^{-5}	3.0789×10^{-4}
8	1.4691×10^{-5}	2.4574×10^{-4}
9	4.71518×10^{-9}	2.2993×10^{-4}
10	4.71518×10^{-9}	2.2571×10^{-4}

Table 2: Values of INQID and INPA

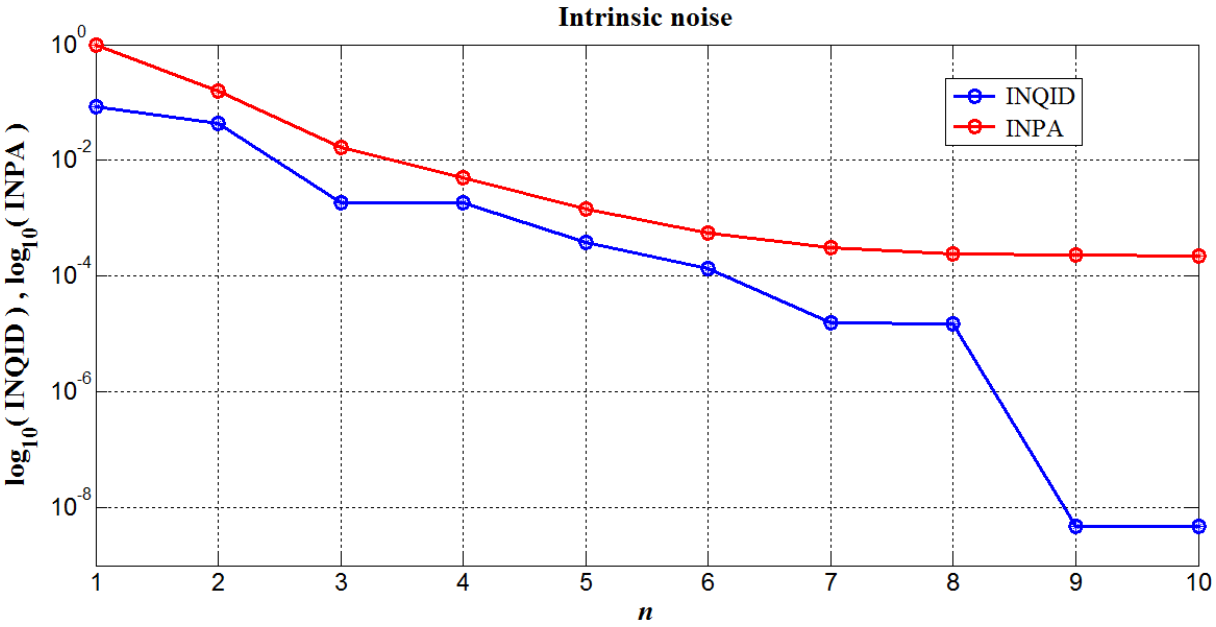

Fig. 18: INQID and INPA for parallel architecture.

VI. Hardware implementation

The serial and parallel architecture have been implemented on an Altera EP3SL150F1152C2 FPGA chip (DE3 board). Hardware test was performed using Agilent equipment. Agilent 16903A logic analysis system generates the digital signal which is the input of the serial or parallel architecture. Agilent 1680A logic analyzer saves in its memory the output signal of the serial or parallel architecture and generates the digital waveform.

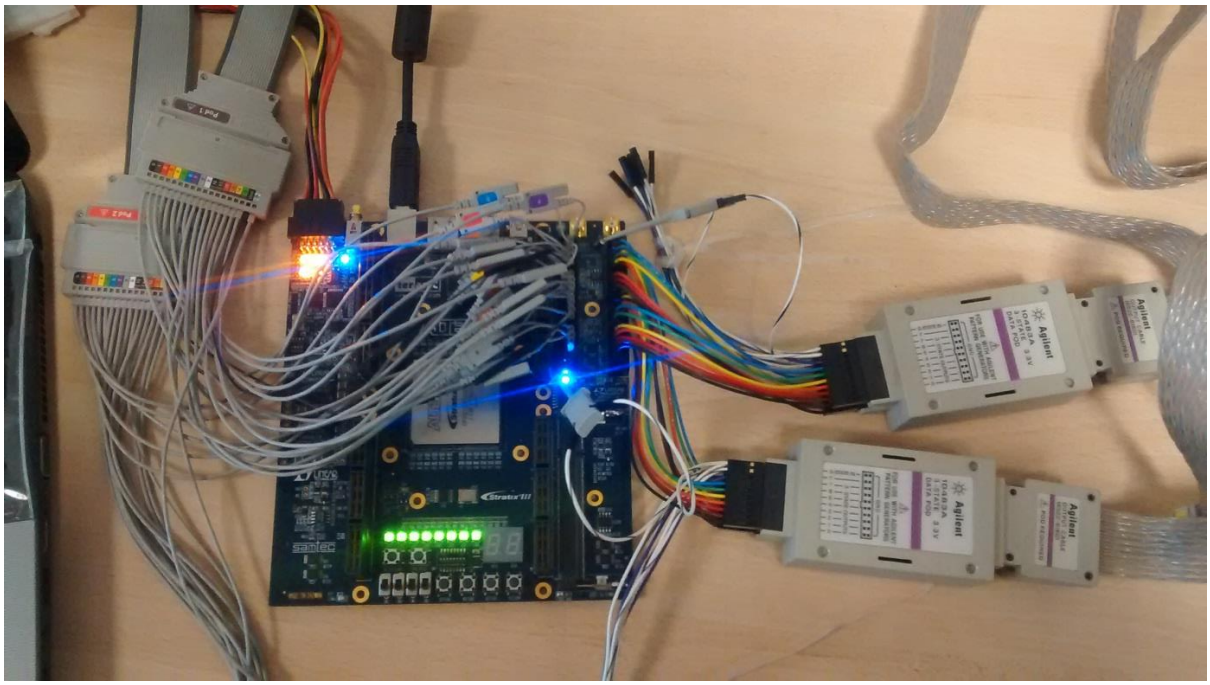

Photo 1: serial architecture.

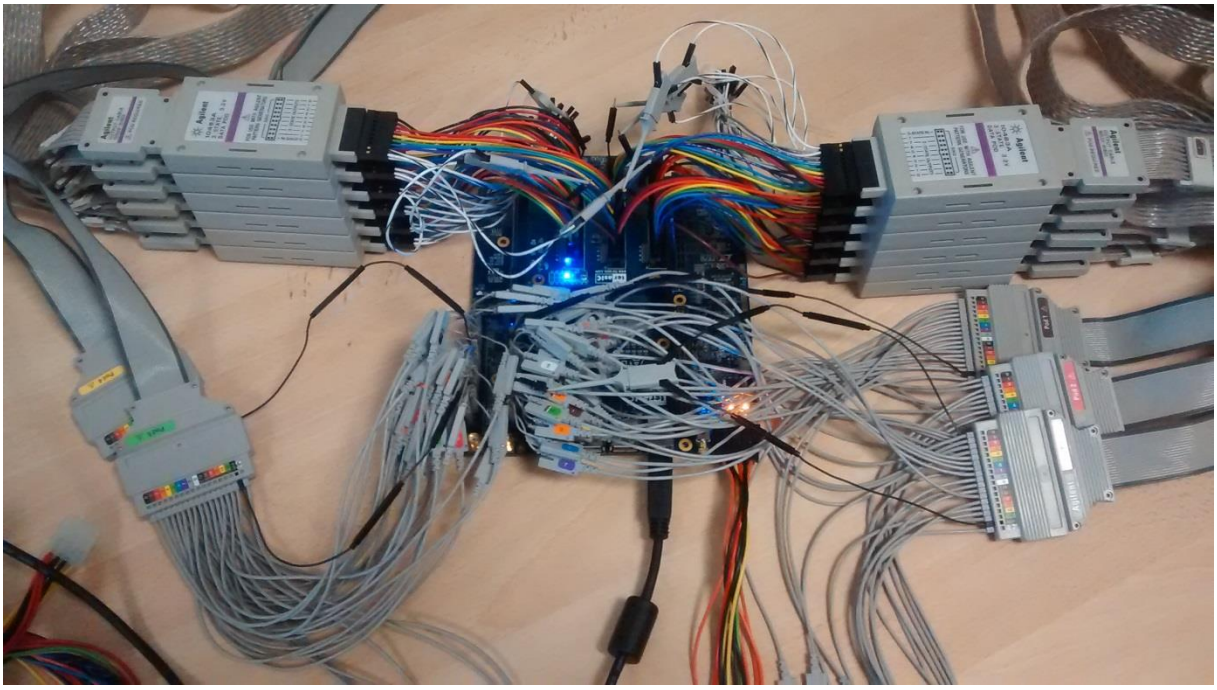

Photo 2: Parallel architecture.

From the memory of Agilent 1680A logic analyzer, the output signal has been analyzed using Matlab, results obtained were identical to results obtained in Matlab simulations and VHDL simulations in ModelSim, thus, with the implementation of the serial and parallel architecture, the design of both architectures is valid and can be used in future generation decoders.

VII. Conclusions

To summarize, this document presents the hardware implementation result of a component performing timing synchronization for large band mono frequency transmission with several type of constellations (BPSK, QPSK, 8PSK, 16APSK, 32APSK and 64APSK). A typical application of the presented design is a receiver for the DVB-S2 and DVB-S2X standards (the only exception is when the roll-off is equal to 0.05, where the observed output Bit Error Rate diverges significantly from the theoretical BER). A serial and a parallel architecture have been developed. The first one is able to support a throughput of 276 Msymbols/s and the later 4×248 = 996 Msymbols/s on an ALTERA STRATIX 3. The serial and parallel architecture work well when the roll-off factor varies between 0.35 downto 0.10, with a transmission clock difference between emitter and receiver of 50 ppm. The output of the Analog Digital Converter requires only a number of quantization bit ***n*** greater than or equal to 7 to obtain almost optimal performance. The hardware complexity depends on the level of parallelism an on the selected FPGA. For an ALTERA STRATIC 3, the required resources of the parallel architecture is 2635 ALUT, 3615 register and 296 DSP block 18-bit elements. Synthesis result has been verified at a rate of 50 MHz using a hardware test platform. Monitored FPGA output shows no divergence with the output generated by the software model.

More information: If you need more information about the work or if you are interested by the algorithm and/or the VHDL code, please, contact Prof. Emmanuel Boutillon at emmanuel.boutillon@univ-ubs.fr

VIII. References

[1] F.M. Gardner, “A BPSK/QPSK Timing-Error Detector for Sampled Receivers”, IEEE Trans. Commun., Vol. COM-34, pp. 423-429, May 1986.

[2] ETSI, “ETSI EN 302 307-1 V1.4.1 (2014-07) Digital Video Broadcasting (DVB) ; Second generation framing structure, channel coding and modulation systems for Broadcasting, Interactive Services, News Gathering and other broadband satellite applications; Part 1: DVB-S2”, 2014.

[3] ETSI, “ETSI EN 302 307-2 V1.1.1 (2014-10) Digital Video Broadcasting (DVB) ; Second generation framing structure, channel coding and modulation systems for Broadcasting, Interactive Services, News Gathering and other broadband satellite applications; Part 2: DVB-S2 Extensions (DVB-S2X)”, 2014.